MEMORY

CONDENSED DATA BOOK

National

Edge Index by Product Family

This is National's Memory condensed databook containing information on MOS and Bipolar Memory Components and Systems. For more detailed information on these products, consult the Memory Data Book or contact a National sales office, representative or distributor.

MOS RAMs 1

Bipolar RAMs 2

CMOS RAMs 3

MOS EPROMs 4

Bipolar PROMs 5

MOS ROMs 6

Bipolar ROMs 7

Shift Registers 8

Memory Systems 9

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

National does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied; and National reserves the right, at any time without notice, to change said circuitry.

© 1977 National Semiconductor

Table of Contents

Edge Index by Product Family I

MOS RAMS SECTION 1

MM1101, MM11011, MM1101A. MM1101A1, MM1101A2 256-Bit (256 x 1) Static . . . . . 1 – 1
MM2101, MM2101-1, MM2101-2 1024-Bit (256 x 4) Static with Sep. I/O . . . . . 1 – 2
MM2102, MM2102-1, MM2102-2 1024-Bit (1024 x 1) Static . . . . . 1 – 3
MM2102A, MM2102AL, 1024-Bit (1024 x 1) Static . . . . . 1 – 4
MM2102MD, MM2102-2MD 1024-Bit (1024 x 1) Static, Mil. Temp. Range . . . . . 1 – 5
MM2111, MM2111-1, MM2111-2 1024-Bit (256 x 4) Static with Common I/O . . . . . 1 – 6
MM2112, MM2112-2 1024-Bit (256 x 4) Static with Common I/O . . . . . 1 – 7
MM2114 4096-Bit (1024 x 4) Static with Common I/O . . . . . 1 – 8
MM4250 256-Bit (256 x 1) Static . . . . . 1 – 1
MM4270 4096-Bit (4096 x 1) TRI-SHARE Port, Dynamic . . . . . 1 – 9
MM4280 4096-Bit (4096 x 1) Dynamic . . . . . 1 – 10
MM5257 4096-Bit (4096 x 1) Static, Fully TTL Compatible . . . . . 1 – 11
MM5269 1024-Bit (256 x 4) Static with On-Chip Registers . . . . . 1 – 12
MM5270 4096-Bit (4096 x 1) TRI-SHARE Port, Dynamic . . . . . 1 – 13
MM5270-5 4096-Bit (4096 x 1) TRI-SHARE Port, Dynamic . . . . . 1 – 14
MM5270A 4096-Bit (4096 x 1) TRI-SHARE Port, Dynamic . . . . . 1 – 15
MM5271A 4096-Bit (4096 x 1) Fully TTL Compatible, Dynamic . . . . . 1 – 16
MM5280 4096-Bit (4096 x 1) Dynamic . . . . . 1 – 17
MM5280-5 4096-Bit (4096 x 1) Dynamic . . . . . 1 – 18
MM5280A 4096-Bit (4096 x 1) Dynamic . . . . . 1 – 19
MM5281 4096-Bit (4096 x 1) Fully TTL Compatible, Dynamic . . . . . 1 – 20
MM5290 16384-Bit (16384 x 1) Fully TTL Compatible, Dynamic . . . . . 1 – 21

BIPOLAR RAMS SECTION 2

DM5489/DM7489 64-Bit (16 x 4) Open Collector . . . . . 2 – 1
DM54LS189/DM74LS189 64-Bit (16 x 4) Low Power TRI-STATE Schottky . . . . . 2 – 2
DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE Schottky . . . . . 2 – 3
DM54S200/DM74S200 256-Bit (256 x 1) TRI-STATE Schottky . . . . . 2 – 4
DM54S206/DM74S206 256-Bit (256 x 1) Open Collector Schottky . . . . . 2 – 5
DM54LS289/DM74LS289 64-Bit (16 x 4) Low Power Open Collector Schottky . . . . . 2 – 6
DM54S289/DM74S289 64-Bit (16 x 4) Open Collector Schottky . . . . . 2 – 7
DM75S68/DM85S68 64-Bit (16 x 4) Schottky Edge-Triggered Register . . . . . 2 – 8
DM7599/DM8599 64-Bit (16 x 4) TRI-STATE . . . . . 2 – 9
DM86S21 64-Bit (32 x 2) Schottky . . . . . 2 – 10
DM93415/DM93415A 1024-Bit (1024 x 1) TTL, Open Collector . . . . . 2 – 11
DM93425/DM93425A 1024-Bit (1024 x 1) TTL, TRI-STATE Output . . . . . 2 – 12
Bipolar RAM Cross Reference Guide . . . . . 2 – 13

CMOS RAMS SECTION 3

MM54C89/MM74C89 64-Bit (16 x 4) TRI-STATE . . . . . 3 – 1
MM54C200/MM74C200 256-Bit (256 x 1) TRI-STATE . . . . . 3 – 2
MM54C910/MM74C910 256-Bit (256 x 1) TRI-STATE . . . . . 3 – 3
MM54C920/MM74C920 1024-Bit(256 x 4) Silicon Gate, 22 Pin . . . . . 3 – 4
MM54C921/MM74C921 1024-Bit Silicon Gate, 18 Pin . . . . . 3 – 4
MM54C929/MM74C929 1024-Bit Silicon Gate, 16 Pin . . . . . 3 – 5
MM54C930/MM74C930 1024-Bit Silicon Gate, 18 Pin . . . . . 3 – 5

MOS EPROMS SECTION 4

MM1702A 2048-Bit (256 x 8) Electrically Programmable and Erasable ROM . . . . . 4 – 1
MM1742 2048-Bit Electrically programmed ROM . . . . . 4 – 2
MM2708, MM2704 8k and 4k UV Erasable (1024 x 8, 512 x 8) PROM . . . . . 4 – 3
MM4203/MM5203 2048-Bit (256 x 8/512 x 4) Electrically Programmable and Erasable ROM . . . . . 4 – 4
MM4243/MM5243 2048-Bit Electrically programmed ROM . . . . . 4 – 5
MM4204/MM5204 4096-Bit (512 x 8) Electrically Programmable and Erasable ROM . . . . . 4 – 6
MM4244/MM5244 4096-Bit Electrically programmed ROM . . . . . 4 – 7

BIPOLAR PROMS SECTION 5

PROM/ROM Selection Guide . . . . . 5 – 1
PROM/ROM Selection Guide . . . . . 5 – 2
DM54S188/DM74S188 256-Bit (32 x 8) Open Collector . . . . . 5 – 3
DM54S288/DM74S288 256-Bit (32 x 8) TRI-STATE . . . . . 5 – 3
DM54S287/DM74S287 1024-Bit (256 x 4) TRI-STATE . . . . . 5 – 4
DM54S387/DM74S387 1024-Bit (256 x 4) Open Collector . . . . . 5 – 4
DM54S470/DM74S470 2048-Bit (256 x 8) Open Collector Schottky . . . . . 5 – 5
DM54S471/DM74S471 2048-Bit (256 x 8) TRI-STATE Schottky . . . . . 5 – 5
DM54S472/DM74S472 4096-Bit (512 x 8) TRI-STATE . . . . . 5 – 6
DM54S473/DM74S473 4096-Bit (512 x 8) Open Collector . . . . . 5 – 6
DM54S570/DM74S570 2048-Bit (512 x 4) Open Collector Schottky . . . . . 5 – 7
DM54S571/DM74S571 2048-Bit (512 x 4) TRI-STATE Schottky . . . . . 5 – 7
DM54S572/DM74S572 4096-Bit (1024 x 4) Open Collector . . . . . 5 – 8
DM54S573/DM74S573 4096-Bit (1024 x 4) TRI-STATE, Schottky . . . . . 5 – 8
DM7577/DM8577 256-Bit (32 x 8) Open Collector . . . . . 5 – 9
DM7578/DM8578 256-Bit (32 x 8) TRI-STATE . . . . . 5 – 10
DM77S221/DM87S221 2048-Bit (256 x 8) Open Collector with Latches . . . . . 5 – 11
DM77S222/DM87S222 2048-Bit (256 x 8) TRI-STATE with Latches . . . . . 5 – 11
DM77S228/DM87S228 8196-Bit (1024 x 8) TRI-STATE . . . . . 5 – 12
DM77S229/DM87S229 8196-Bit (1024 x 8) Open Collector . . . . . 5 – 12
DM77S295/DM87S295 4096-Bit (512 x 8) Open Collector . . . . . 5 – 13
DM77S296/DM87S296 4096-Bit (512 x 8) TRI-STATE . . . . . 5 – 13
Bipolar PROM Cross Reference Guide . . . . . 5 – 14
PROM Programming procedure . . . . . 5 – 15

MOS ROMS SECTION 6

MM2316A 16384-Bit (2048 x 8) read only memory . . . . . 6 – 1
MM2316E 16384-Bit (2048 x 8) read only memory . . . . . 6 – 2
MM3501 1024-Bit (128 x 8) Mask Programmable . . . . . 6 – 3
MM4210/MM5210 1024-Bit (256 x 4) Mask Programmable . . . . . 6 – 4
MM4211/MM5211 1024-Bit (256 x 4) Mask Programmable . . . . . 6 – 5
MM5212 12288-Bit (1k x 12) Mask Programmable . . . . . 6 – 6
MM4213/MM5213 2048-Bit (256 x 8/521 x 4) Mask Programmable . . . . . 6 – 7
MM4214/MM5214 4096-Bit (512 x 8) Mask Programmable . . . . . 6 – 8
MM5215 12288-Bit (1k x 12) Mask Programmable . . . . . 6 – 9
MM4220/MM5220 1024-Bit (128 x 8/256/4) Mask Programmable . . . . . 6 – 10
MM4221/MM5221 1024-Bit (128 x 8/256 x 4) Mask Programmable . . . . . 6 – 11
MM4229/MM5229 3072-Bit (256 x 12) Mask Programmable . . . . . 6 – 12
MM4230/MM5230 2048-Bit (256 x 8/512 x 4) Mask Programmable . . . . . 6 – 13
MM4231/MM5231 2048-Bit (256 x 8/512 x 4) Mask Programmable . . . . . 6 – 14
MM4232/MM5232 4096-Bit (512 x 8/1k x 4) Mask Programmable . . . . . 6 – 15
MM4233/MM5233 4096-Bit (512 x 8) Mask Programmable . . . . . 6 – 16
MM4240/MM5240 2560-Bit (62-8 x 5) Static Character Generator . . . . . 6 – 17
MM4241/MM5241 3072-Bit (64 x 6 x 8) Mask Programmable . . . . . 6 – 18
MM4242/MM5242 8192-Bit (1024 x 8) Mask Programmable . . . . . 6 – 19
MM4246/MM5246 16384-Bit (2048 x 8) Mask Programmable . . . . . 6 – 20
SK0003 Sine/Cosine Look-Up Table . . . . . 6 – 21

BIPOLAR ROMS SECTION 7

DM54187/DM74187 1024-Bit (256 x 4) Mask Programmable . . . . . 7 – 1
DM54L187A/DM74L187A 1024-Bit (256 x 4) Low Power Open Collector Mask Programmable . . . . . 7 – 2
DM54S270/DM74S270 2048-Bit (512 x 4) Open Collector Schottky Mask Programmable . . . . . 7 – 3
DM54S271/DM74S271 2048-Bit (256 x 8) Open Collector Schottky Mask Programmable . . . . . 7 – 4
DM54S370/DM74S370 2048-Bit (512 x 4) TRI-STATE Schottky Mask Programmable . . . . . 7 – 3
DM54S371/DM74S371 2048-Bit (256 x 8) TRI-STATE Schottky Mask Programmable . . . . . 7 – 4
DM75S28/DM85S28 8192-Bit (1024 x 8) TRI-STATE Schottky Mask Programmable . . . . . 7 – 5
DM75S29/DM85S29 8192-Bit (1024 x 8) Open Collector Schottky Mask Programmable . . . . . 7 – 5
DM7575/DM8575 Mask Programmable Logic Array . . . . . 7 – 6
DM7576/DM8576 Mask Programmable Logic Array . . . . . 7 – 6
DM7596/DM8596 4096-Bit (512 x 8) TRI-STATE Mask Programmable . . . . . 7 – 7
DM7597/DM8597 1024-Bit (256 x 4) TRI-STATE Mask Programmable . . . . . 7 – 8
DM75S97/DM85S97 1024-Bit (256 x 4) TRI-STATE Schottky Mask Programmable . . . . . 7 – 9
DM7598/DM8598 256-Bit (32 x 8) TRI-STATE Mask Programmable . . . . . 7 – 10

DM8678 Bipolar Character Generator (5 x 7) or (7 x 9) . . . . . 7 – 11
DM76L97/86L97 1024-Bit (256 x 4) TRI-STATE Low Power Mask Programmable . . . . . 7 – 12
DM77S201/DM87S201 2048-Bit (256 x 8) Open Collector with Latches Mask Programmable . . . . . 7 – 13
DM77S202/DM87S202 2048-Bit (256 x 8) TRI-STATE With Latches Mask Programmable . . . . . 7 – 13
DM77S95/DM87S95 4096-Bit (512 x 8) Open Collector Schottky Mask Programmable . . . . . 7 – 14
DM7796/DM8796 4096-Bit (512 x 8) TRI-STATE Mask Programmable . . . . . 7 – 7
DM77S96/DM87S96 4096-Bit (512 x 8) TRI-STATE Schottky Mask Programmable . . . . . 7 – 14

SHIFT REGISTERS SECTION 8

MM1402A Quad 256-Bit Dynamic . . . . . 8 – 1
MM1403A Dual 512-Bit Dynamic . . . . . 8 – 1
MM1404A 1024-Bit Dynamic . . . . . 8 – 1
MM5024A 1024-Bit Dynamic . . . . . 8 – 1
MM4025/MM5025 Dual 1024-Bit Dynamic . . . . . 8 – 2
MM4026/MM5026 Dual 1024-Bit Dynamic . . . . . 8 – 2
MM4027/MM5027 2048-Bit Dynamic . . . . . 8 – 2
MM5054 Dual 64/72/80-Bit Static . . . . . 8 – 3
MM4055/MM5055 Quad 128-Bit Static . . . . . 8 – 4
MM4056/MM5056 Dual 256-Bit Static . . . . . 8 – 4
MM4057/MM5057 512-Bit Static . . . . . 8 – 4
MM5058 1024-Bit Static . . . . . 8 – 5
MM5060 Dual 144-Bit Mask Programmable Static . . . . . 8 – 6
MM5061 Quad 100-Bit Static . . . . . 8 – 7

MEMORY SYSTEMS SECTION 9

Memory Systems . . . . . 9 – 1
NS3-1 Bulk Storage Memory . . . . . 9 – 3
NS11 Memory Series . . . . . 9 – 5
NS11/03 Memory Card . . . . . 9 – 6
NS21 Memory Card . . . . . 9 – 7
NS32 Memory Card . . . . . 9 – 8
NS400-N Series Memory Card . . . . . 9 – 9
NS400-C Series Memory Card . . . . . 9 – 10
NS3000-1 Memory Card . . . . . 9 – 11

MOS RAMs

MM1101, MM11011, MM1101A, MM1101A1, MM1101A2, MM4250
256-bit fully decoded static random access memory

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply voltages.

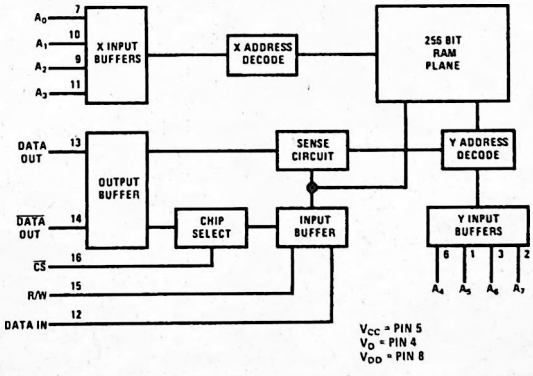
features

- Fast access times MM1101A2 500 ns max
  MM11011, MM1101A1 1.0 μs max
  MM1101, MM1101A 1.5 μs max
  MM4250 650 ns max
- Improved speed/power product MM1101A2 1/3 of 1101A
- Low power operation 1.5 mW/bit
- Fewer system components – bipolar compatible input and output
- Second source flexibility – MM1101, MM1101A MM11011, MM1101A1 second sources available
- TRI-STATE™ output – wired OR capability
- Specified ambient temperature 0°C to +70°C, for MM1101 family; −55°C to +125°C for MM4250

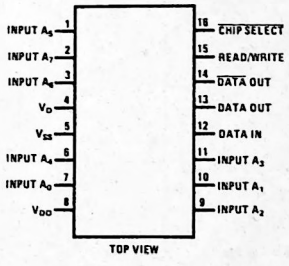
applications

- High speed buffer memories
- Local memory store

block and connection diagrams



Dual-In-Line Package



Order Number MM1101D, MM1101AD, MM1101A1D, MM1101A2D, MM11011D or MM4250D
See Package 3

Order Number MM1101N, MM1101AN, MM1101A1N, MM1101A2N or MM11011N
See Package 15

MM2101, MM2101-1, MM2101-2 1024-bit (256 × 4) static MOS RAM with separate I/O

general description

The National MM2101 is a 256 word by 4 bit static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data.

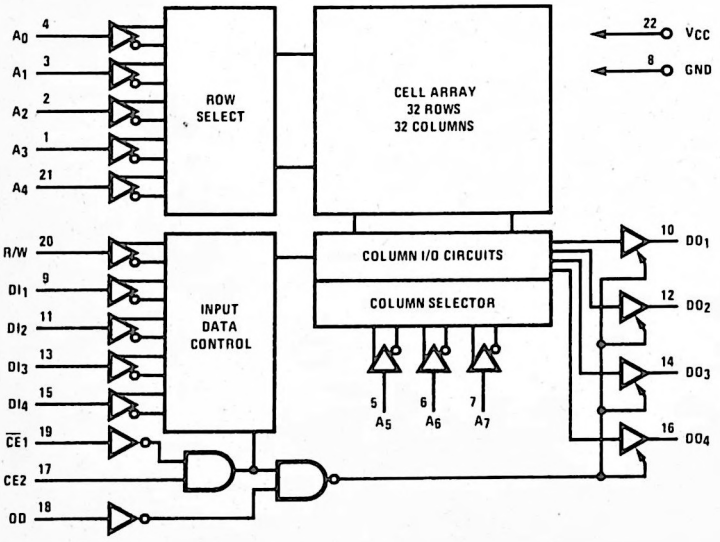
The 2101 is directly TTL compatible in all respects: inputs, outputs, and a single +5 V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

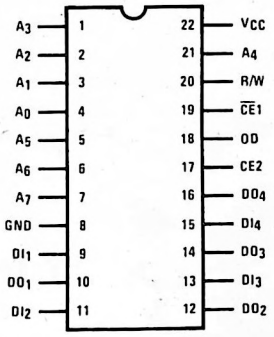
National's silicon gate technology also provides protection against contamination, and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time — 0.5 to 1.0 μs Max.
- Single +5 V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required.
- Simple Memory Expansion — Chip Enable Input
- Low Cost Packaging — 22 Pin Epoxy B Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Tri-State ® Output — OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

block and connection diagrams





PIN NAMES

DI_1 - DI_4	DATA INPUT
A_0 - A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}1$, CE2	CHIP ENABLE
OD	OUTPUT DISABLE
DO_1 - DO_4	DATA OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2101D, MM2101-1D or MM2101-2D
See Package 5

Order Number MM2101-N, MM2101-1N or MM2101-2N
See Package 17

MOS RAMs

MM2102, MM2102-1, MM2102-2
1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

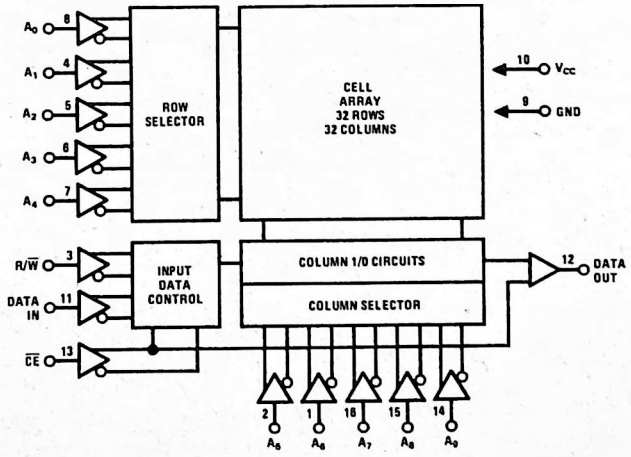
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input (CE) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

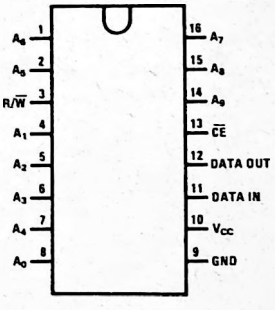
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 150 mW typ
- Fast access
  - MM2102 1μs
  - MM2102-1 500 ns
  - MM2102-2 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- Low cost 16-pin Epoxy B package

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2102D, MM2102-1D or MM2102-2D
See Package 3

Order Number MM2102N, MM2102-1N or MM2102-2N
See Package 15

MM2102A, MM2102AL family
1024-bit (1024 × 1) static random access memories

general description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories are manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

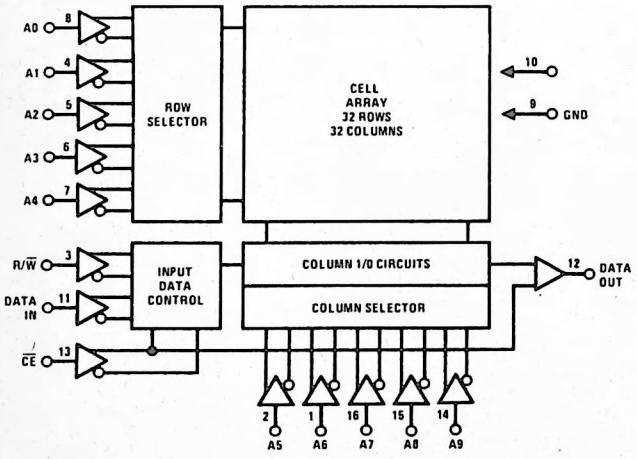
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

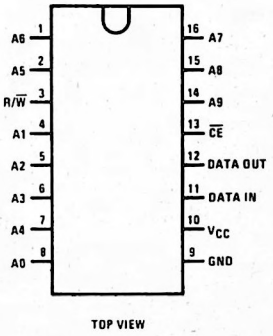
features

- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

block diagram

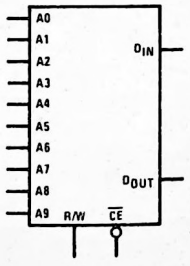


connection diagram



TOP VIEW

logic symbol



MOS RAMs

MM2102MD, MM2102-2MD military temperature range 1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

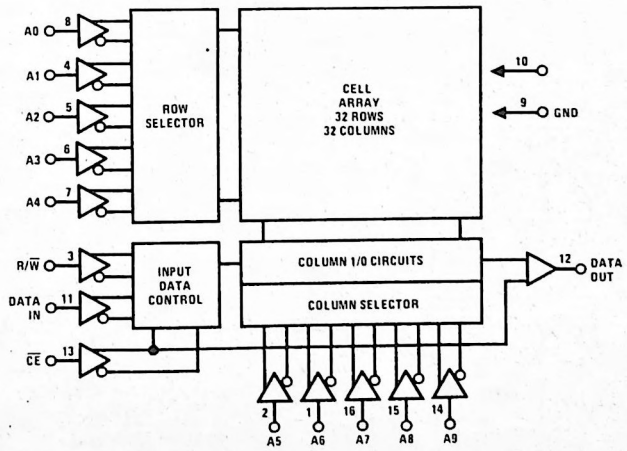
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

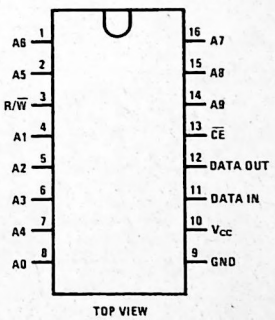
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power 150 mW typ
- Fast Access
  - MM2102 1μs
  - MM2102-2 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- −55°C to +125°C Operation

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2102MD or MM2102-2MD
See Package 3

MM2111, MM2111-1, MM2111-2 1024-bit (256 × 4) static MOS RAM with common I/O and output disable

general description

The National MM2111 is a 256 by 4 static random access memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

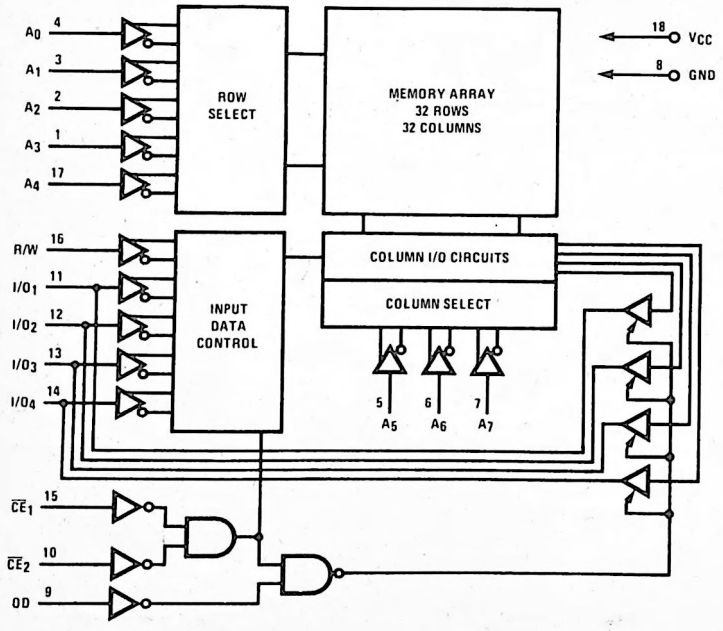
The 2111 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The two Chip-enables allow easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

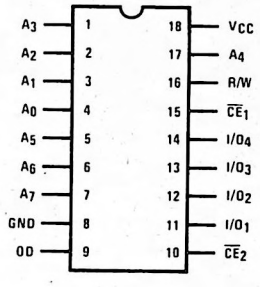
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 0.5 to 1.0 μs Max.
- Simple Memory Expansion — Chip Enable Input
- Low Cost Packaging — 18 Pin Epoxy B Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Tri-State ® Output — OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}1$	CHIP ENABLE 1
$\overline{CE}2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

Order Number MM2111D, MM2111-1D or MM2111-2D
See Package 4
Order Number MM2111N, MM2111-1N or MM2111-2N
See Package 16

MM2112, MM2112-2 1024-bit (256 × 4) static MOS RAM with common data I/O

general description

The National MM2112 is a 256 by 4 static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

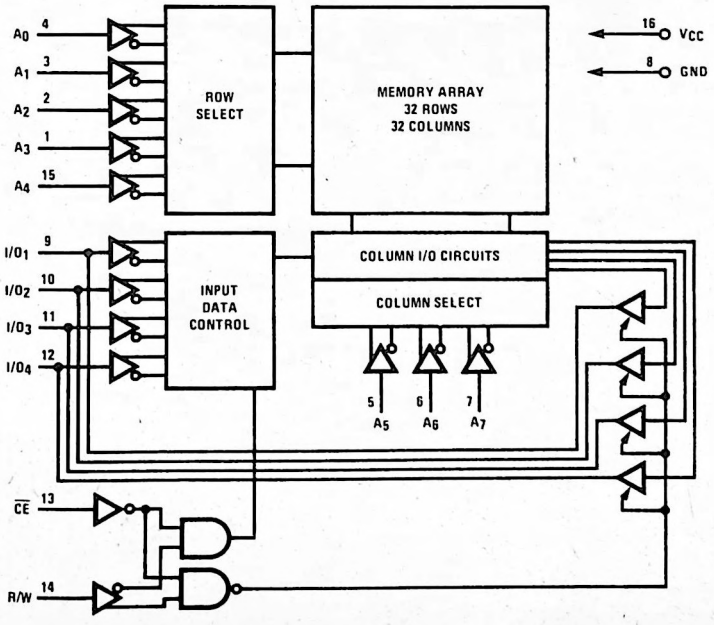
The MM2112 is directly TTL in all respects: inputs, outputs and a single +5 V supply. The Chip-enable allows easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

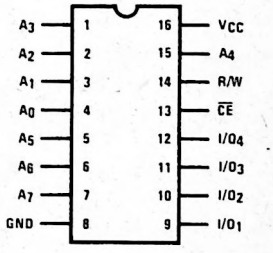
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5 V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 0.65 to 1 μs Max.
- Simple Memory Expansion — Chip Enable Input
- Low Cost Packaging — 16 Pin Epoxy B Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Tri-State ® Output — OR-Tie Capability

block and connection diagrams





PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2112D
or MM2112-2D
See Package 3

Order Number MM2112N
or MM2112-2N
See Package 15

Preliminary

MM 2114 4K (1024 x 4 BIT) STATIC RAM

GENERAL DESCRIPTION

The MM2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout - in both the array and the decoding - and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

The MM2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The MM2114 is placed in a 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

FEATURES

Hihg Density 18 Pin Package

Access Time 200ns Typical

Identical Cycle and Access Times

Low Operating Power Dissipation 250mW typical

Single +5V Supply

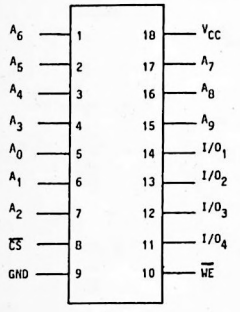
No Clock or Timing Strobe Required

Completely Static Memory

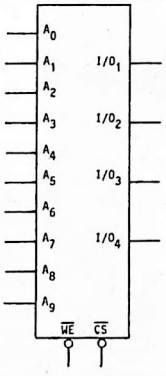
Directly TTL Compatible:All Inputs and Outputs

Common Tri-State Data I/O

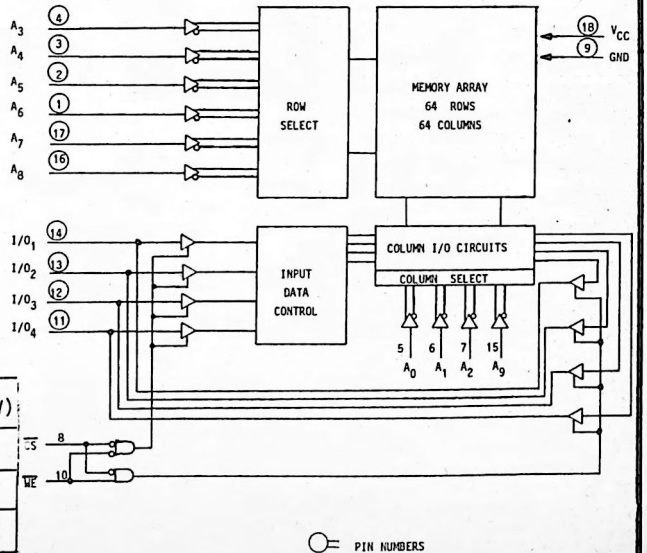
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1-I/O_4	DATA INPUT/OUTPUT		

MM4270 TRI-SHARE™ extended temperature range 4096-bit dynamic random access read/write memory

general description

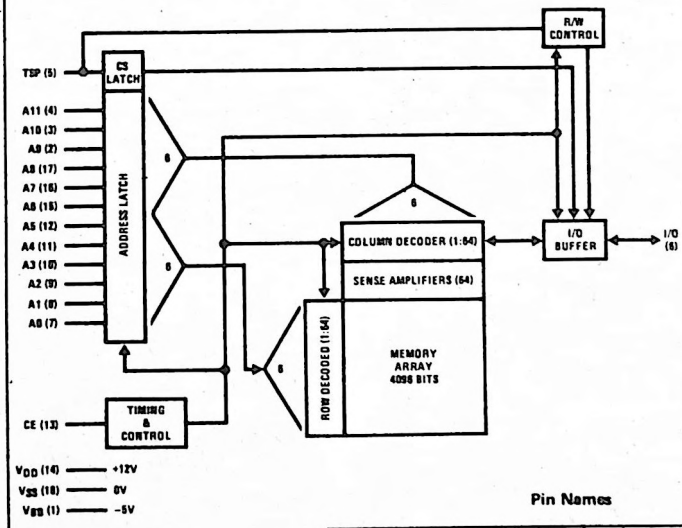
The MM4270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

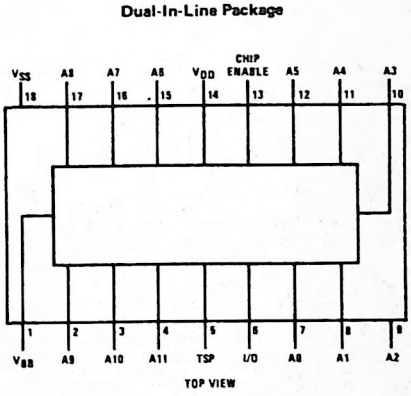
The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM4270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

features

- 4096 x 1 bit organization
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams





Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0–A5

SEPTEMBER 1976

MM 4280 4096 -bit dynamic random access read/write memory with extended temperature range

general description

National's MM4280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM4280 must be refreshed every 1 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh. Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

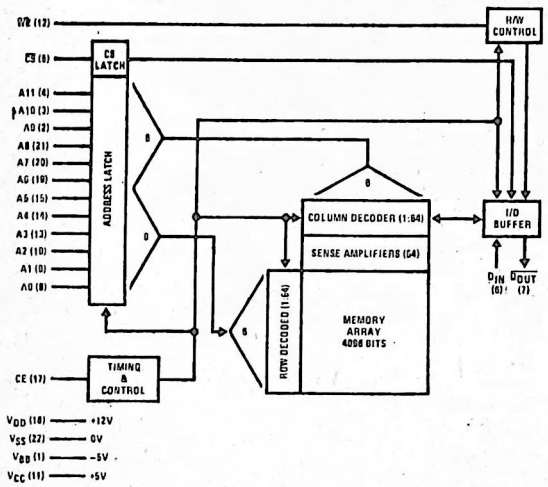
The MM4280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM4280 uses a single transistor cell to minimize the device area.

The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Extended temperature range: −55°C to +85°C
- Organization: 4096 x 1
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and outputs
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

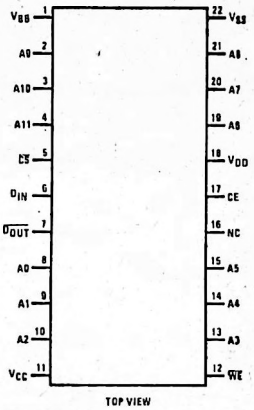
block diagram



Memory Inverts From Data In to Data Out

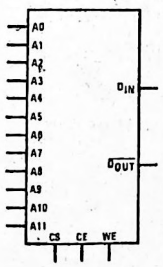
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Pin Numbers

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

MM 5257

4K (4096 x 1) Fully TTL Compatible Random Access Memory

GENERAL DESCRIPTION

The MM5257 is a 4096 word by 1 bit static random access memory fabricated using N-Channel silicon gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

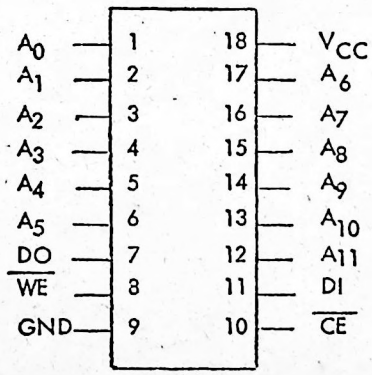
The separate chip enable input (CE) controlling the TRI-STATE output allows easy memory expansion by OR-tying individual devices to a data bus.

The output is also Tri stated during write to simplify common I/O applications.

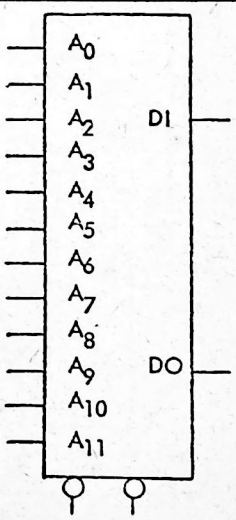
FEATURES

- All inputs and outputs directly DTL/TTL compatible
- Static operation - no clocks or refreshing required
- Low Power - 250mW typical
- High Speed - 200ns typical
- TRI - STATE output for bus interface
- Separate I/O
- Single +5V supply

BLOCK AND CONNECTION DIAGRAM



TOP VIEW
MM5257



LOGIC SYMBOL
MM5257

MM5269 1024-bit (256 × 4) fully decoded static RAM with on chip registers

general description

The National MM5269 is a 256 word x 4 bit Static Random Access Memory device fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. Data in and data out have the same polarity.

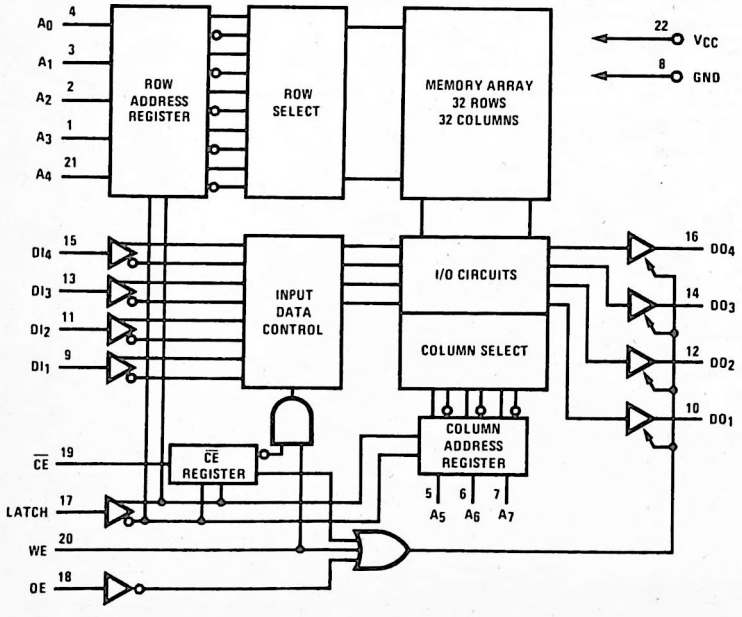
The MM5269 is fully TTL compatible including inputs, outputs and power supply. The chip enable input allows memory expansion and the address latch feature eliminates the need for external address registers. The output enable is provided for systems which use a common input/output data bus. All of the features of this memory device can be combined to make a low cost, high performance and easy to manufacture memory system. System design costs are also minimized because of the ease-of-use of the MM5269.

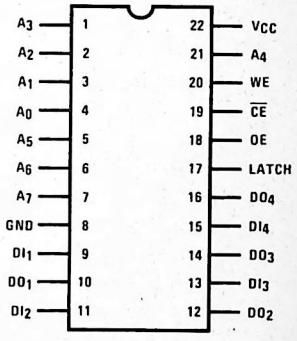
National's Silicon Gate process provides protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs
- On Chip Address and Chip Enable Registers
- Directly TTL Compatible – All Inputs and Outputs
- Single +5 V Power Supply
- Tri-State ® Output – OR-Tie Capability
- Output Enable for Common Data Bus Systems
- Static Memory – No Refresh Required
- Packaged in a 22 Pin Epoxy B Dual-In-Line

block and connection diagrams





Order Number MM5269D
See Package 5
Order Number MM5269N
See Package 17

MM5270 TRI-SHARE™ 4096-bit fully decoded dynamic random access read/write memory

general description

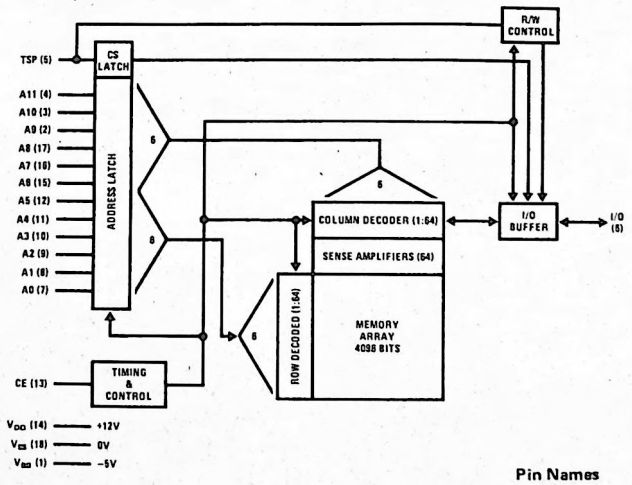
The MM5270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

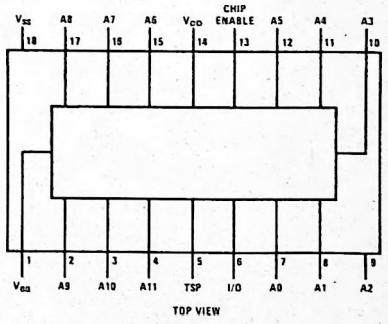
features

- 4096 x 1 bit organization
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5270D
See Package 4

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	D_{IN}/D_{OUT}		

*Refresh Addess A0–A5

MM5270-5 TRI-SHARE™ 4096-bit random access read/write memory

general description

The MM5270-5 is a slower speed version of National's MM5270 dynamic RAM. Please refer to the MM5270 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

Order Number MM5270D-5
See Package 4

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 470 ns, t_{CE} = 300 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 300 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

National Semiconductor

MOS RAMs

MM5270A 4096-Bit Dynamic Random Access Memory

General Description

The MM5270A is a 4096-bit dynamic random access memory with TRI-SHARE®. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read, write and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port: thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5270A goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected, but it will be refreshed if the chip enable clock is pulsed.

The RAM must be refreshed every 2 ms. This can be accomplished by performing a cycle at each of the 64 row addresses (A0–A5).

Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

Features

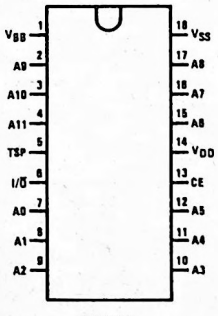
- Pin compatible with MM5270
- Standard power supplies, 12V, 5V, −5V
- Easy system interface
  - One high level input—chip enable
  - All other pins TTL compatible
- TRI-STATE® output
- Organized 4096 x 1
- Inputs protected against static charge
- Simple Read-Modify-Write operation
- Address and chip select registers on-chip
- Industry standard 22-pin DIP
- Non-latching D_{IN} input simplifies write and RMW timing
- Access time
  - MM5270A: 150 ns
  - MM5270A-12: 125 ns
  - MM5270A-10: 100 ns

  Cycle time, Read, Write, Read-While-Write
  - MM5270A: 280 ns
  - MM5270A-12: 245 ns
  - MM5270A-10: 210 ns

  Cycle time, Read-Modify-Write
  - MM5270A: 330 ns
  - MM5270A-12: 285 ns
  - MM5270A-10: 240 ns

Connection Diagram

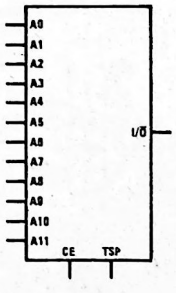
Dual-In-Line Package



TOP VIEW

Order Number MM5270AD
See Package 4
Order Number MM5270AJ
See Package 10A
Order Number MM5270AN
See Package 16

Logic Symbol



Pin Names

*A0–A11	Address Inputs	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Row address A0–A5

National Semiconductor

MOS RAMs

MM5271A TRI-SHARE™ 4096-Bit Fully TTL Compatible Dynamic Random Access Read/Write Memory

General Description

The MM5271A is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read, write, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/$\overline{O}$. When the MM5271A goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected, but it will be refreshed if the chip enable clock is pulsed.

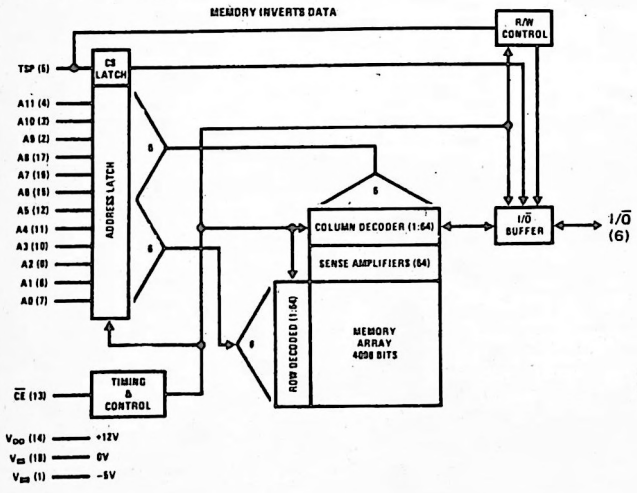
The RAM must be refreshed every 2 ms. This can be accomplished by performing a cycle at each of the 64 row addresses (A0–A5).

Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

Features

- 4096 x 1 bit organization
- Access time—115 ns max MM5271A-1
  140 ns max MM5271A
- Cycle time—215 ns min MM5271A-1
  260 ns min MM5271A
- TRI-SHARE port
- High memory density—18-pin package
- All pins TTL compatible
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

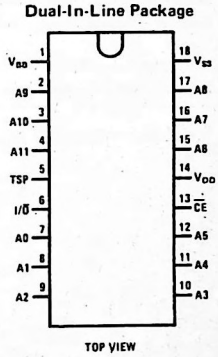
Block Diagram



Connection Diagram

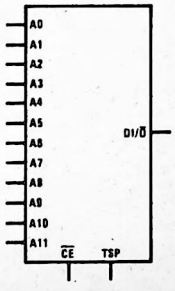
Dual-In-Line Package

Order Number MM5271AD
See Package 4
Order Number MM5271AJ
See Package 10A
Order Number MM5271AN
See Package 16



TOP VIEW

Logic Symbol



Pin Names

*A0–A11	Address Inputs	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/$\overline{O}$	$D_{IN}/\overline{D_{OUT}}$		

*Row address A0–A5

MM5280 4096-bit dynamic random access memory

general description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

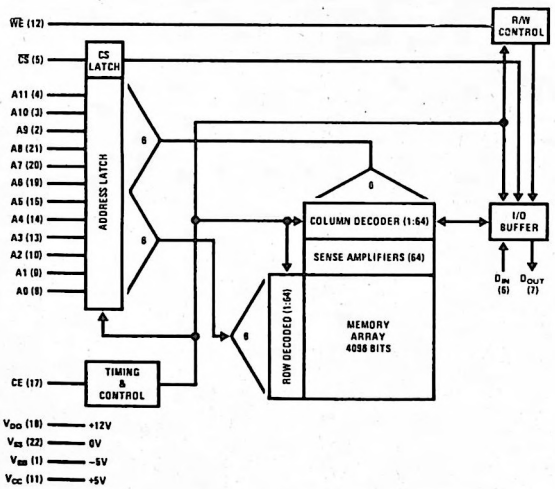
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

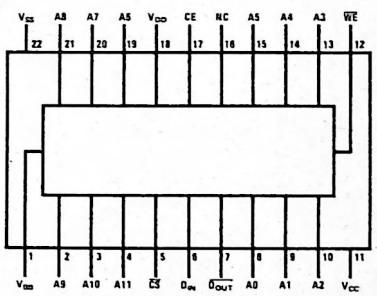
features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5280D
See Package 5

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

MM5280-5 4096-bit dynamic random access read/write memory

general description

The MM5280-5 is a slower speed version of National's MM5280. Please refer to the MM5280 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Order Number MM5280D-5
See Package 5

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

National Semiconductor

MOS RAMs

MM5280A 4096-Bit Dynamic Random Access Memory

General Description

National's MM5280A is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The RAM must be refreshed every 2 ms. This can be accomplished by performing a cycle at each of the 64 row addresses (A0–A5).

Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

The MM5280A has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280A uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

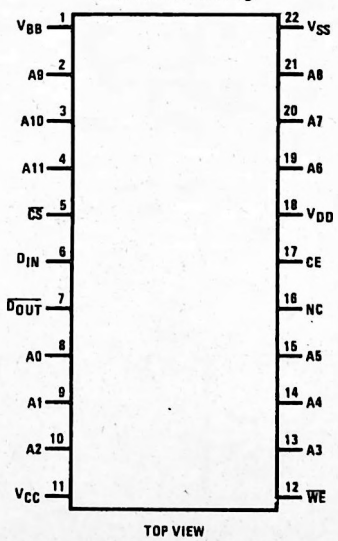
In every cycle where Chip Select is active ($\overline{CS}$ low), regardless of when or if the Write pulse occurs, previous data contained by the addressed cell will appear on $D_{\overline{OUT}}$ at t_{ACC}. This unique feature allows Read-While-Write cycles to be performed using minimum Write cycle timing.

Features

- Pin compatible with MM5280
- Standard power supplies, 12V. 5V. –5V
- Easy system interface
  - One high level input—chip enable
  - All other pins TTL compatible
- TRI-STATE® output
- Organized 4096 x 1
- Inputs protected against static charge
- Simple Read-Modify-Write operation
- Read-While-Write capability
- Address and chip select registers on-chip
- Industry standard 22-pin DIP
- Non-latching D_{IN} input simplifies write and RMW timing
- Access time
  - MM5280A: 150 ns
  - MM5280A-2: 125 ns
  - MM5280A-1: 100 ns
  - Cycle time, Read, Write, Read-While-Write
    - MM5280A: 280 ns
    - MM5280A-2: 245 ns
    - MM5281A-1: 210 ns
  - Cycle time, Read-Modify-Write
    - MM5280A: 330 ns
    - MM5280A-2: 285 ns
    - MM5280A-1: 240 ns

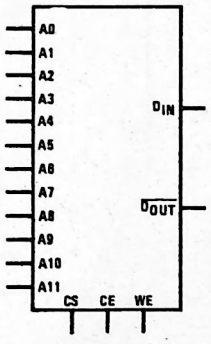
Connection Diagram and Logic Symbol

Dual-In-Line Package



TOP VIEW

Order Number MM5280AD
See Package 4
Order Number MM5280AN
See Package 17
Order Number MM5280AJ
See Package 10B



Pin Names

*A0–A11	Address Inputs	V_{BB}	Power (–5V)
CE	Chip Enable	V_{CC}	Power (5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (12V)
D_{IN}	Data Input	V_{SS}	Ground
$D_{\overline{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Row address A0–A5

MM5281 4096-bit fully TTL compatible dynamic random access memory

general description

National's MM5281 is a 4096 word by 1 bit fully TTL compatible dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM5281 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

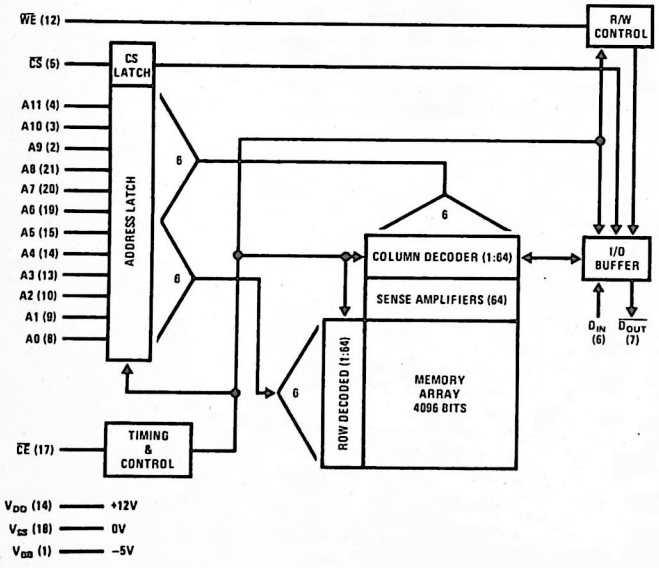
The MM5281 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5281 uses a single transistor cell to minimize the device area.

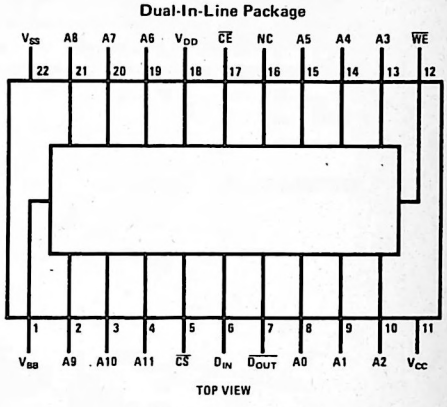
The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Organization: 4096 x 1
- Access time 250 ns maximum
- Cycle time 400 ns minimum
- TTL compatible
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams





Order Number MM5281D
See Package 5

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

National Semiconductor

MOS RAMs

PRELIMINARY

MM5290 16,384 × 1 Bit Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

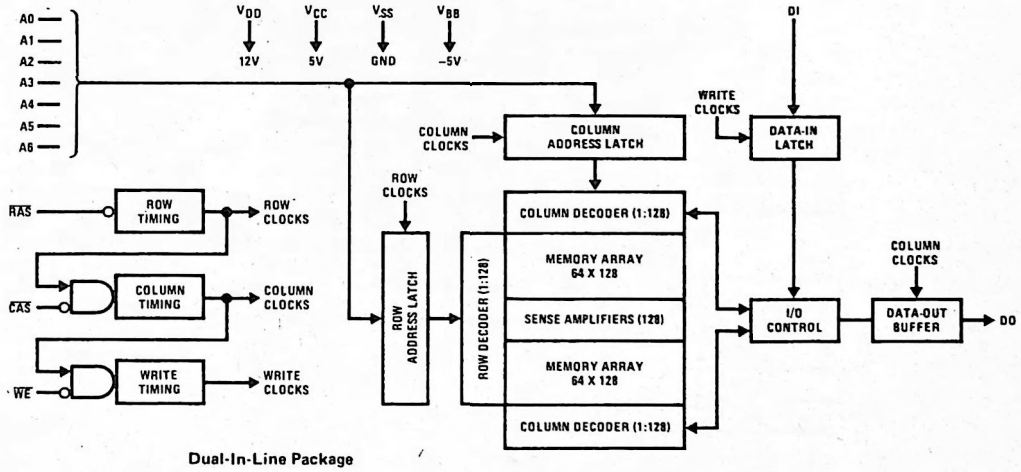
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including an RAS-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

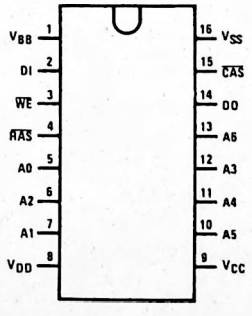
Features

- Access times:150 ns, 200 ns, 300 ns
- Low power:462 mW max
- TTL compatible: all inputs and output
- Gated CAS—noncritical timing
- Read, Write, Read-Modify-Write and RAS-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5290J
See Package 10

Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0—A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Bipolar RAMs

DM5489/DM7489 (SN5489/SN7489)
64-bit random access read/write memory

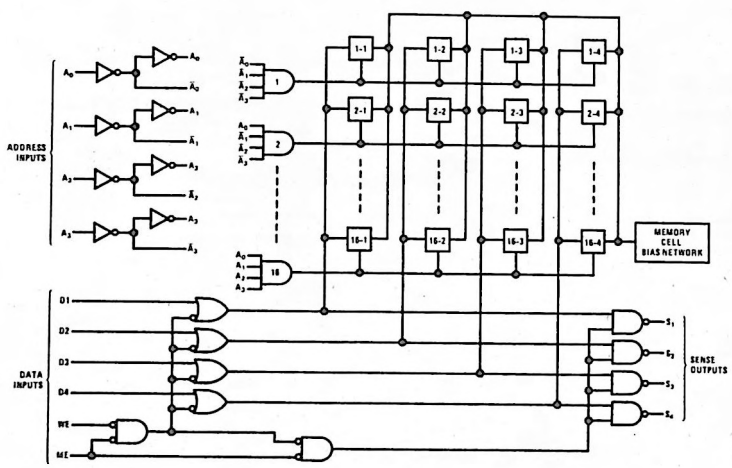
general description

The DM5489/DM7489 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

features

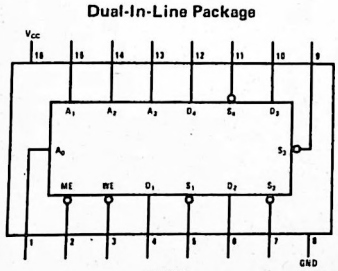
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 23 ns
- Typical access 35 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

block diagram



connection diagram

Dual-In-Line Package



Order Number DM5489J or DM7489J
See Package 10

Order Number DM7489N
See Package 15

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

DM54LS189/DM74LS189 low power 64-bit random access memories with TRI-STATE® outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip enable input to simplify decoding required to achieve the desired system organization. This device is implemented with low power Schottky technology resulting in one-fifth power while retaining the speed of standard TTL.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM54LS289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip enable input and the read/write input are low. While the read/write input is low, the outputs are in the high impedance state. When a number of the DM54LS189 outputs are bus-connected, this high impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

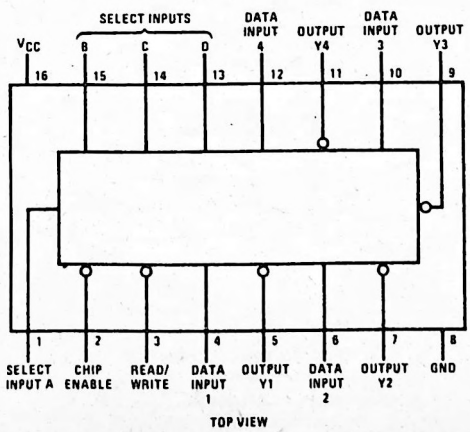
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip enable is low. When the chip enable input is high, the outputs will be in the high impedance state.

features

- Schottky-clamped for high speed applications
  - Access from chip enable input—40 ns typ
  - Access from address inputs—60 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- Low power—75 mW typ
- DM54LS189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level
L = low level
X = don't care

DM54S189/DM74S189 64-bit random access memories with TRI-STATE® outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector DM54S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM54S189 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

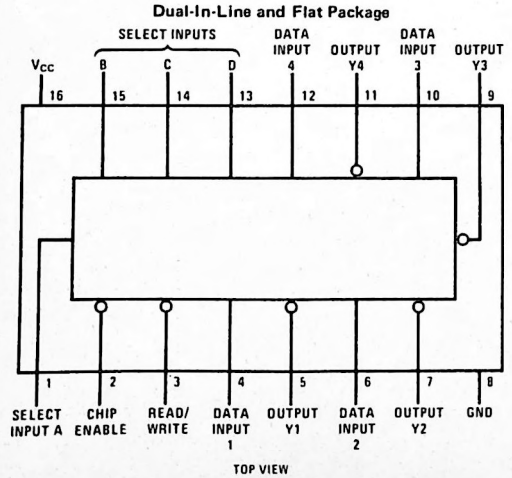
The fast access time of the DM54S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189 outputs being at a high impedance during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  - access from chip-enable input 12 ns typ
  - access from address inputs 25 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM54S289, DM74S289 are functionally equilvalent, have open-collector outputs, and are compatible with Intel 3101A in most applications
- DM54S189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = High Level
L = Low Level
X = Don't Care

Order Number DM54S189J or DM74S189J
See Package 10
Order Number DM74S189N
See Package 15

Bipolar RAMs

DM54S200/DM74S200 256-bit read/write schottky memories with TRI-STATE® outputs

general description

The DM54S200/DM74S200 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output.

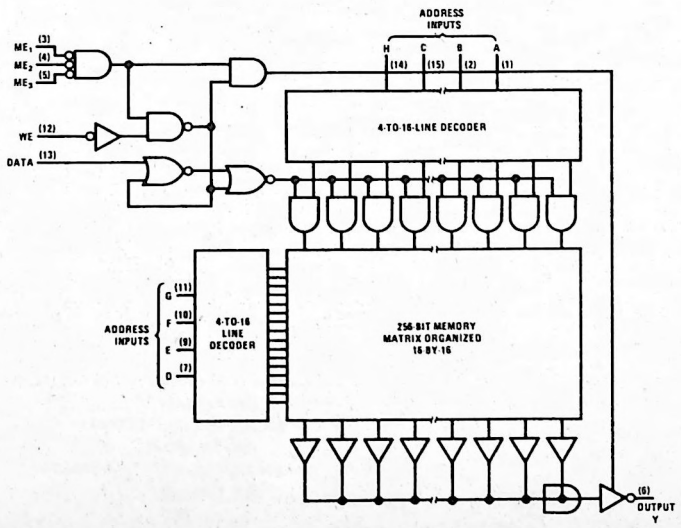
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

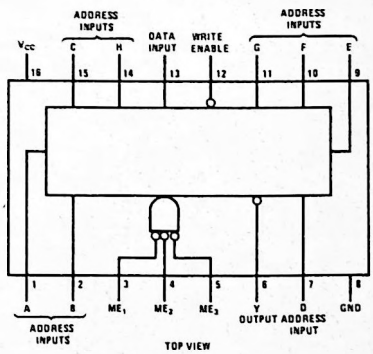
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 20 ns typ
  - Access from address inputs 31 ns typ
  - Power dissipation 1.7 mW/bit typ
- TRI-STATE output for driving bus-organized systems and/or highly capacitive loads
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line and Flat Package



Order Number DM54S200J
or DM74S200J
See Package 10

Order Number DM74S200N
See Package 15

Order Number DM54S200W
or DM74S200W
See Package 28

DM54S206/DM74S206 256-bit read/write schottky memories with open-collector outputs

general description

The DM54S206/DM74S206 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

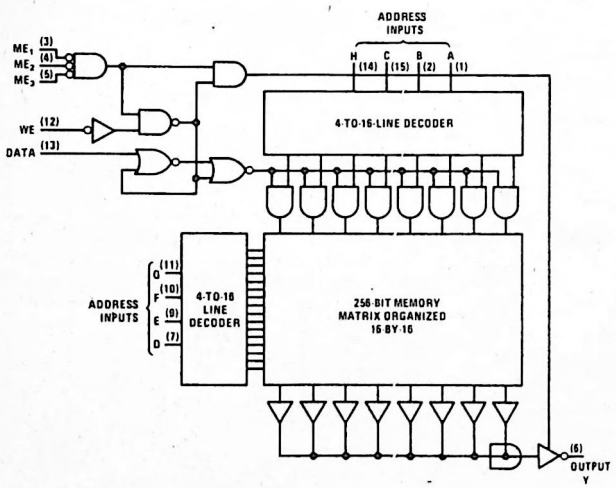
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is off.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be off.

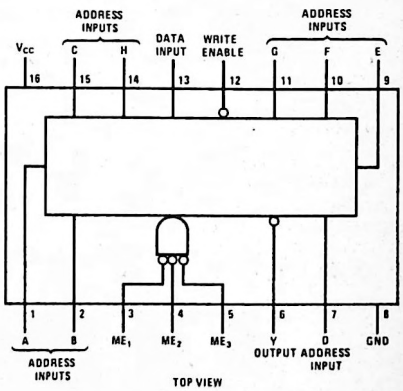
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 17 ns typ
  - Access from address inputs 35 ns typ
  - Power dissipation 1.4 mW/bit typ
- Open-collector output for word expansion
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line and Flat Package



Order Number DM54S206J or DM74S206J
See Package 10

Order Number DM74S206N
See Package 15

Order Number DM54S206W or DM74S206W
See Package 28

National Semiconductor

Bipolar RAMs

PRELIMINARY

DM54LS289/DM74LS289 low power 64-bit random access memories with open-collector outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip enable input to simplify decoding required to achieve the desired system organization. This device is implemented with low power Schottky technology resulting in one-fifth power while retaining the speed of standard TTL.

The open-collector outputs are ideal for controlled-impedance bus lines.

The unique functional capability of the DM54LS289 outputs being at a high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-logic level (OFF).

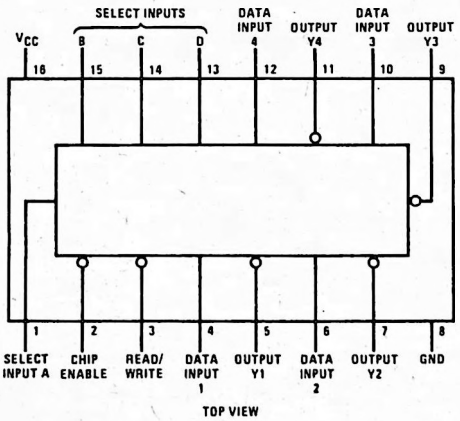
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs are high (OFF).

features

- Schottky-clamped for high speed applications
  - Access from chip enable input—40 ns typ
  - Access from address inputs—60 ns typ
- Open-collector outputs for controlled-impedance bus lines
- DM54LS189/DM74LS189 are functionally equivalent, but have TRI-STATE® outputs
- DM54LS289 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



Order Number DM54LS289J or DM74LS289J
See Package 10
Order Number DM74LS289N
See Package 15
Order Number DM54LS289W
See Package 28

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level
L = low level
X = don't care

DM54S289/DM74S289 64-bit random access memories with open-collector outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-logic level ("OFF").

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs are high ("OFF").

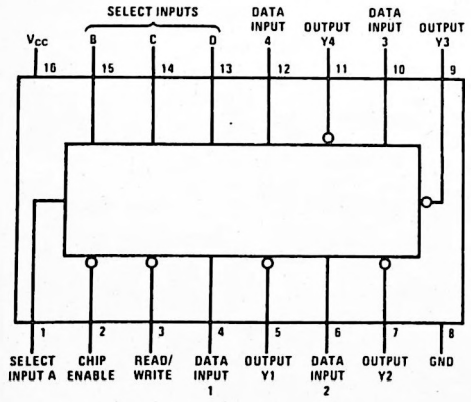
The fast access time of the DM54S289 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The unique functional capability of the DM54S289 outputs being at a high during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  Access from chip-enable 12 ns typ
  Access from address inputs 25 ns typ
- Open collector outputs for controlled-impedance bus lines
- DM54S189/DM74S189 are functionally equivalent, but have TRI-STATE® outputs
- DM54S289 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding
- Compatible with Intel 3101A in most applications

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S289J or DM74S289J
See Package 10
Order Number DM74S289N
See Package 15

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = High Level
L = Low Level
X = Don't Care

Bipolar RAMs

DM75S68/DM85S68 64-bit (16×4) edge triggered register

general description

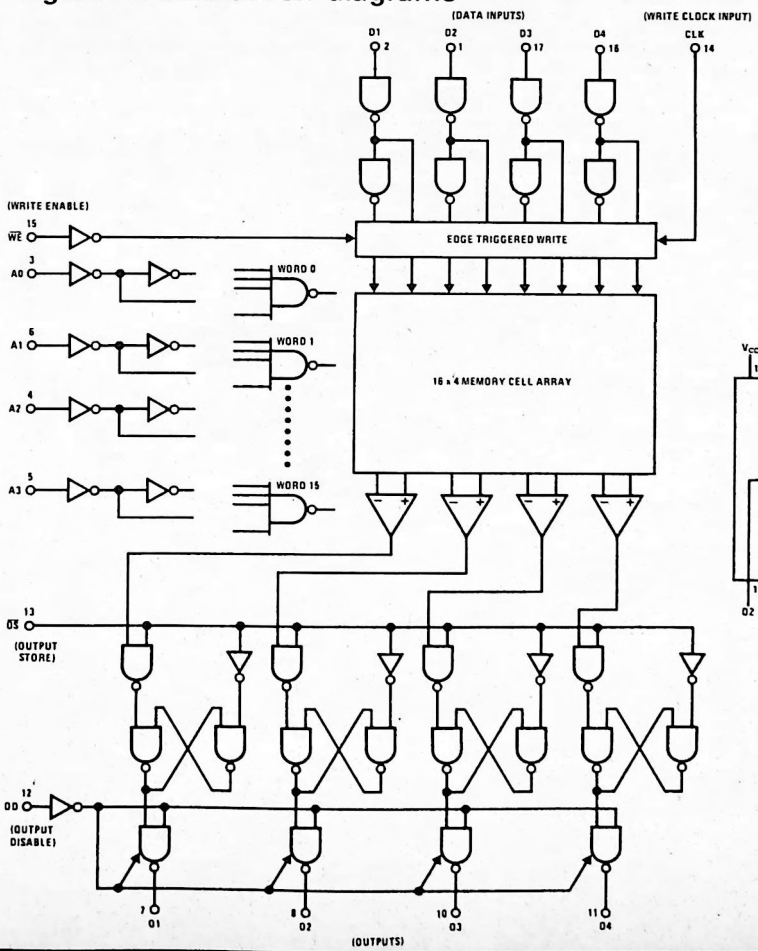
The DM75S68/DM85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

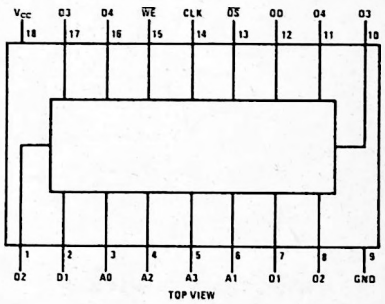
features

- On chip output register
- Edge triggered write
- High speed — 30 ns typ
- TRI-STATE output
- Optimized for register stack applications
- Typical power dissipation — 350 mW
- 18-pin package

logic and connection diagrams



Dual-In-Line Package



Order Number DM75S68D
or DM85S68D
See Package 4

Order Number DM85S68N
See Package 16

DM7599/DM8599 TRI-STATE™
64-bit random-access read/write memory

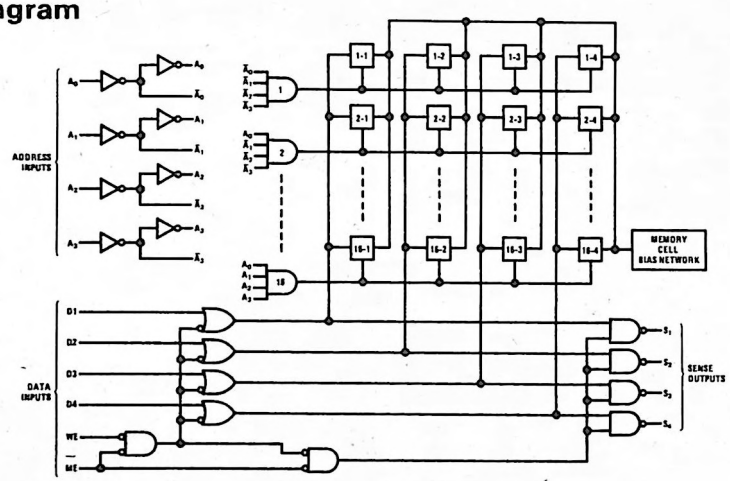
general description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

features

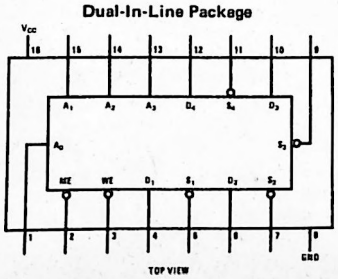
- Series 54/74 compatible
- Same pin-out as SN5489/SN7489
- Organized as 16 4-bit words
- Expandable to 2048 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns
- Typical power dissipation 400 mW

block diagram



connection diagram

Dual-In-Line Package



Order Number DM7599J
or DM8599J
See Package 10

Order Number DM8599N
See Package 15

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

Bipolar RAMs

DM86S21 64-bit bipolar high speed RAM (32 × 2 RAM)

general description

The DM86S21 is a TTL 64-bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The DM86S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5 input decoder when the Read-Write enable input, CE is at logic "1." $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. $\overline{C}$ is the write control input. When $\overline{W_X}$ and $\overline{C}$ are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or $\overline{C}$ is at logic "1."

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, $\overline{L}$, is logic "1" and data is being read from the DM86S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When $\overline{L}$ goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When $\overline{L}$ goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

features

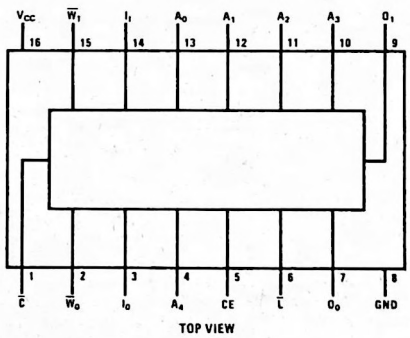
- Buffered address lines
- On chip latches
- On chip decoding
- Bit masking control lines
- Enable control line
- Open collector outputs with 40 mA capability
- Protected inputs
- Very high speeds 25 ns (typ)
- Second source to Signetics 82S21

applications

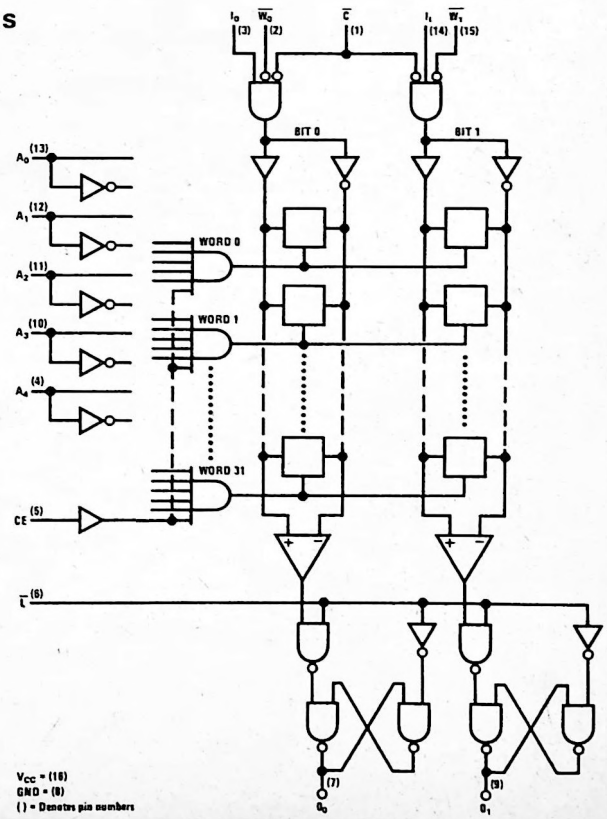
- Scratch pad memory
- Buffer memory
- Accumulator register
- Control store

logic and connection diagrams

Dual-In-Line Package



Order Number DM86S21J
See Package 10
Order Number DM86S21N
See Package 15



Preliminary

DM93415, DM93415A TTL 1024 × 1-bit fully decoded random access memories

general description

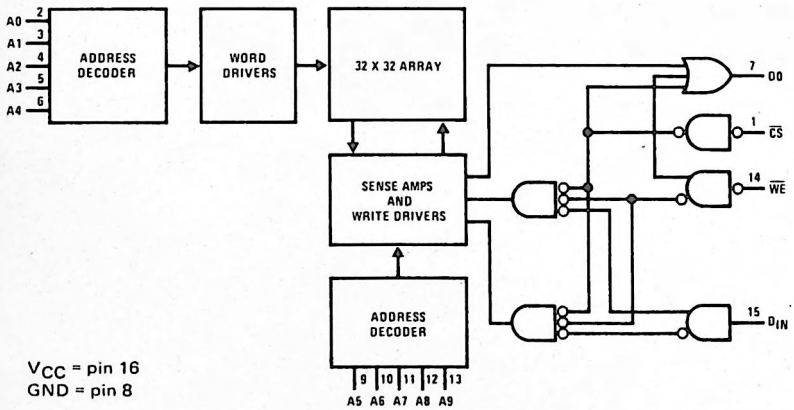
The DM93415 and DM93415A are 1024-bit read/write Random Access Memories organized 1024 words by 1-bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical access times of 40 ns for the DM93415 and 30 ns for the DM93415A.

The DM93415 and DM93415A include full decoding on-chip, separate data input and data output lines and an active low chip select. They are fully compatible with standard DTL and TTL logic families and have an uncommitted collector output for ease of memory expansion.

features

- Uncommitted collector output
- TTL inputs and output
- Non-inverting data output
- Organized 1024 words by 1-bit
- Typical read access time
  - DM93415A commercial—30 ns
  - DM93415 commercial—40 ns
  - DM93415 military—40 ns
- Chip select access time—15 ns typ
- Power dissipation -0.5 mW/bit typ
- Power dissipation decreases with increasing temperature

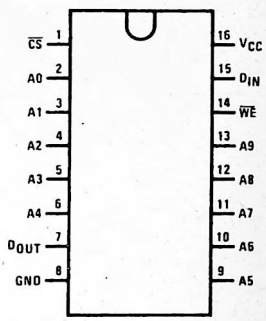
logic diagram



V_{CC} = pin 16
GND = pin 8

connection diagram

Dual-In-Line and Flat Package

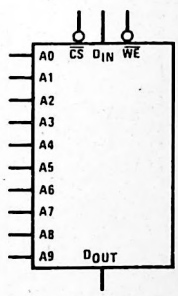


TOP VIEW

Pin Description

$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

logic symbol



National Semiconductor

Bipolar RAMs

PRELIMINARY

DM93425, DM93425A TTL 1024 × 1-bit fully decoded random access memories

general description

The DM93425 and DM93425A are 1024-bit read/write Random Access Memories organized 1024 words by 1-bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical address access times of 40 ns for the DM93425 and 30 ns for the DM93425A.

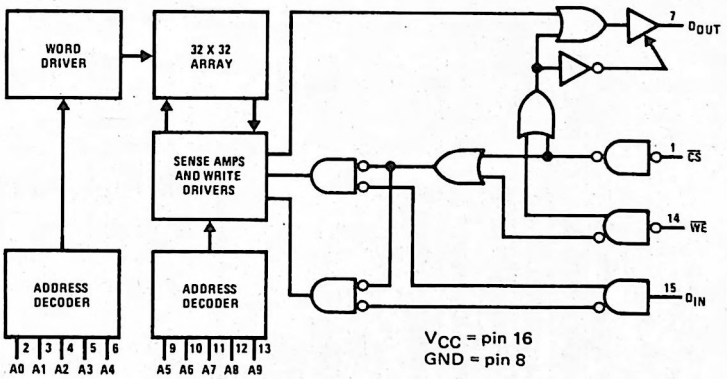
The DM93425 and DM93425A include full decoding on-chip, separate data input and data output lines and an active low chip select and write enable. They are fully compatible with standard DTL and TTL logic families. A TRI-STATE® output is provided to drive bus organized systems and/or highly capacitive loads.

features

- TRI-STATE output
- Organized 1024 words by 1-bit
- TTL inputs and output—full 16 mA drive capability
- Typical read access time
  - DM93425A commercial—30 ns
  - DM93425 commercial—40 ns
  - DM93425 military—40 ns
- Chip select access time—15 ns typ
- Non-inverting data output
- Power dissipation—0.5 mW/bit typ
- Power dissipation decreases with increasing temperature

2

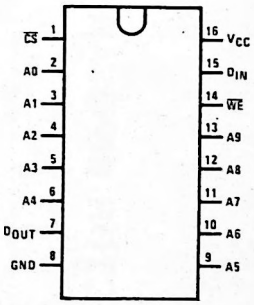
logic diagram



V_{CC} = pin 16
GND = pin 8

connection diagram

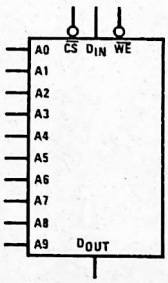
Dual-In-Line Package



TOP VIEW

Order Number DM93425J or DM93425AJ
See Package 10

logic symbol



Pin Description

$\overline{CS}$	Chip Select
A0—A9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

NATIONAL SEMICONDUCTOR BIPOLAR RAM CROSS REFERENCE GUIDE

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	F.S.C. M = MIL C = COM	INTEL M = MIL P = COM	INTERSIL M = MIL P = COM	MMI MIL/COM	SIGNETICS S = MIL N = COM	T.I. MIL/COM
64-Bit (16 x 4)	OC	DM5489/DM7489	AM3101		3101	IM5501		8225	SN5489/7489
	TS	DM7599/DM8599							
High Speed 64-Bit (16 x 4)	OC	DM54S289/DM74S289	AM27S02	93403	3101A		5560/6560	82S25	SN54S289/74S289
	TS	DM54S189/DM74S189	AM27S03				5561/6561		SN54S189/74S189
Low Power 64-Bit (16 x 4)	OC	DM54LS289/DM74LS289	AM27LS02				L5560/L6560		
	TS	DM54LS189/DM74LS189	AM27LS03				L5561/L6561		
File Reg. (16 x 4)	TS	DM75S68/DM85S68							
256-Bit (256 x 1)	OC	DM54S206/DM74S206	AM27S01	93411 93411A	3107 3107A	IM5533A	5530/6530	82S07 82S17 82S117	SN54S301/74S301
	TS	DM54S200/DM74S200	AM27S00	93421 93421A	3106 3106A	IM5523A	5531/6531	82S06 82S16 82S116	SN54200/74200 SN54S200/74S200 SN54S201/74S201
1024-Bit (1024 x 1)	OC	DM93415AM/DM93415AC		93415 93415A		IM5508 IM5508A		82S10	SN54S309/74S309
	TS	DM93425AM/DM93425AC		93425 93425A		IM5518 IM5518A		82S11	SN54S209/74S209

CMOS RAMs

MM54C89/MM74C89 64-bit TRI-STATE® random access read/write memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

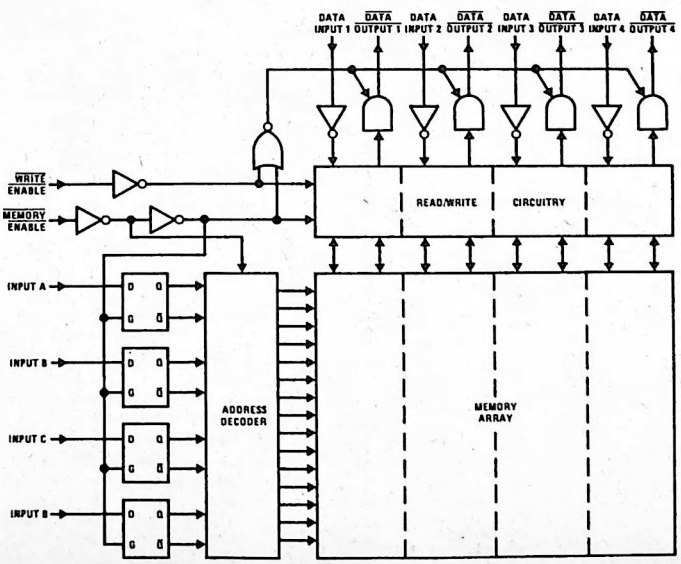
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

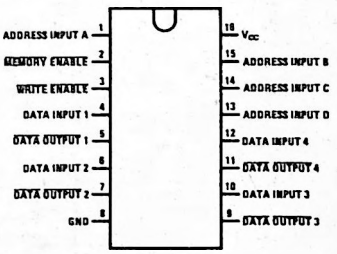
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams





TOP VIEW

Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

MM54C200/MM74C200 256-bit TRI-STATE® random access read/write memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a $\overline{\text{write enable}}$ line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the $\overline{\text{memory enable}}$ must occur for the memory to be selected.

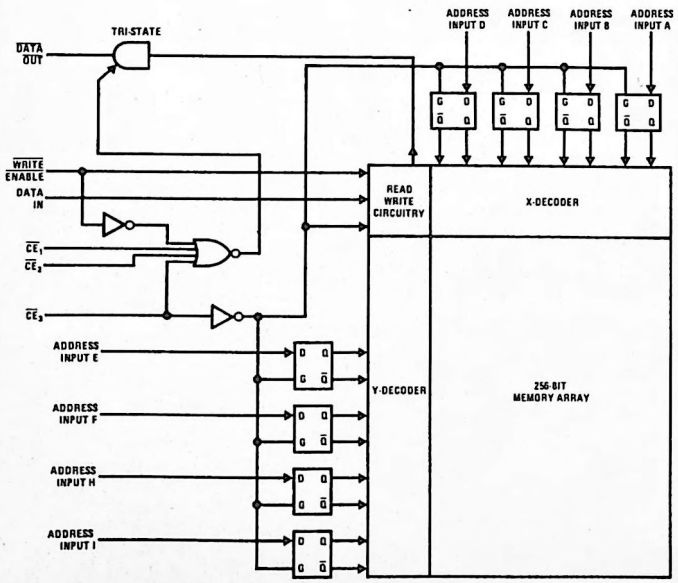
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{\text{write enable}}$ high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

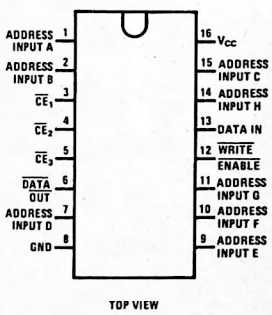
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{\text{write enable}}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{\text{write enable}}$ low.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

logic and connection diagrams





TOP VIEW

Order Number MM54C200D or MM74C200D
See Package 3
Order Number MM74C200N
See Package 15

MM54C910/MM74C910 256-bit TRI-STATE® random access read/write memory

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for t_{WE} and data must remain stable t_{HD} after write enable returns high.

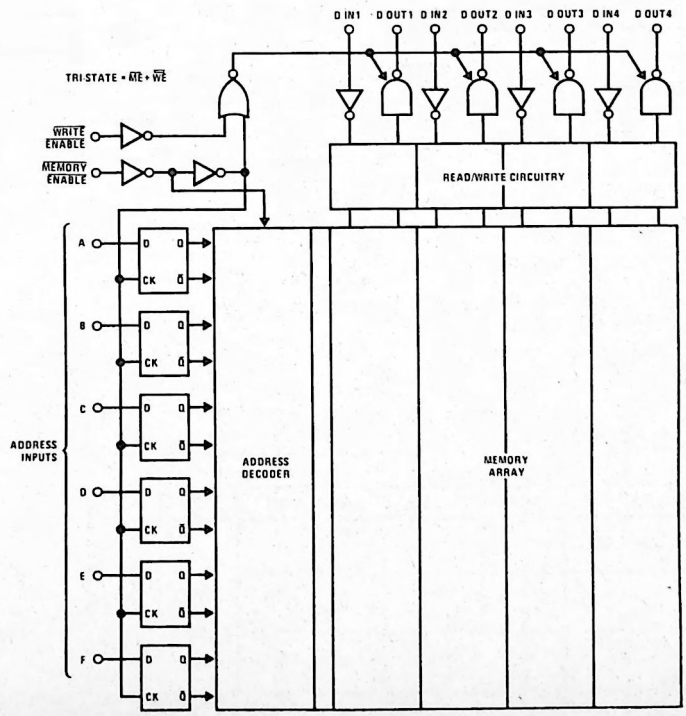
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

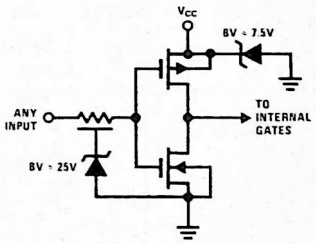
features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

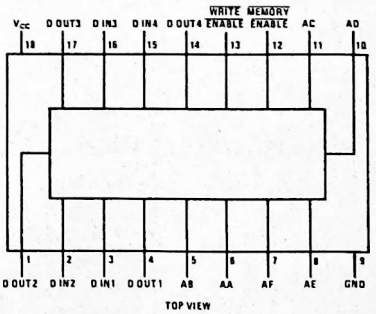
logic and connection diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910D or MM74C910D
See Package 4
Order Number MM74C910N
See Package 16

National Semiconductor

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

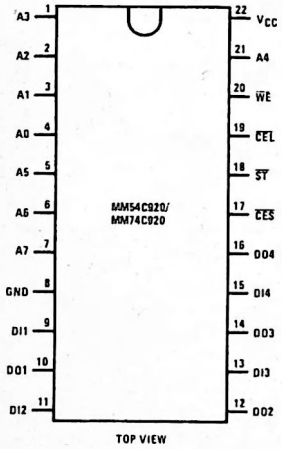
Complete address decoding as well as 2-chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C920–3 MM74C921–3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

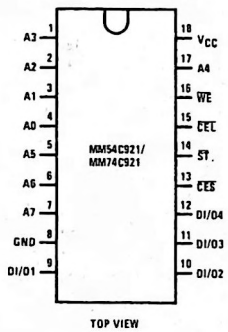
Connection Diagrams

Dual-In-Line Package



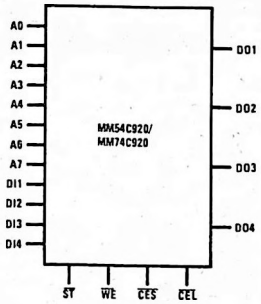
TOP VIEW

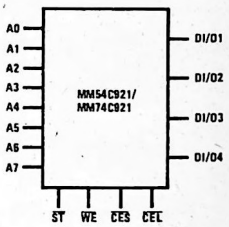
Dual-In-Line Package



TOP VIEW

Logic Symbols





Ordering Information

	MILITARY	COMMERCIAL	PACKAGE*
MM54C920, MM54C921	X		J, D
MM74C920, MM74C921		X	N, J, D
MM74C920–1, MM74C921–3		X	N, J, D

*J and N package available mid-1977

MM54C929/MM74C929, MM54C930/MM74C930 1024-bit static silicon gate CMOS RAMs

general description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon gate CMOS technology. These RAMS are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, three chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input.

Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor minicomputer and main frame memory applications.

features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

block and connection diagrams

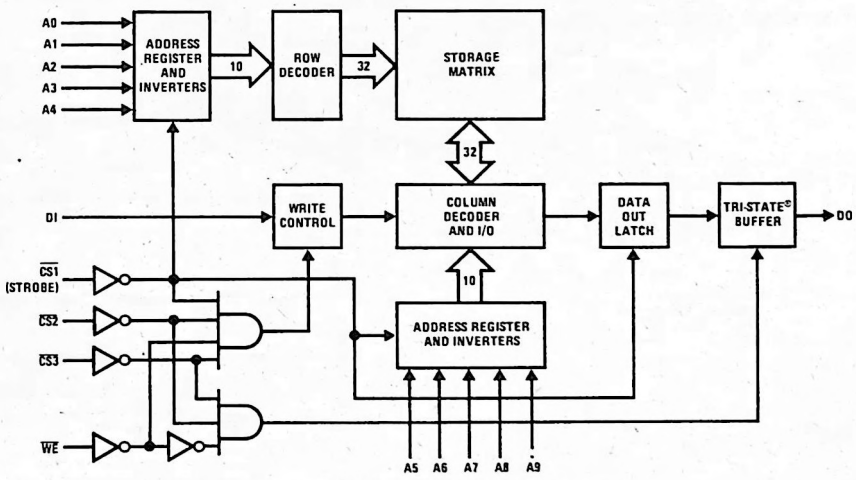
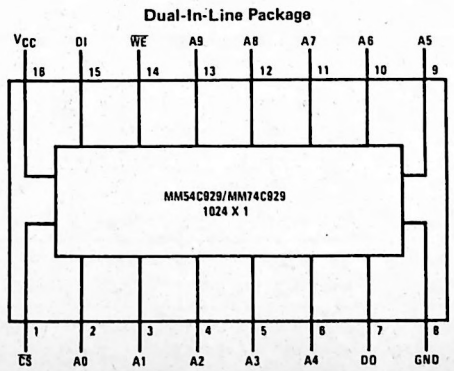
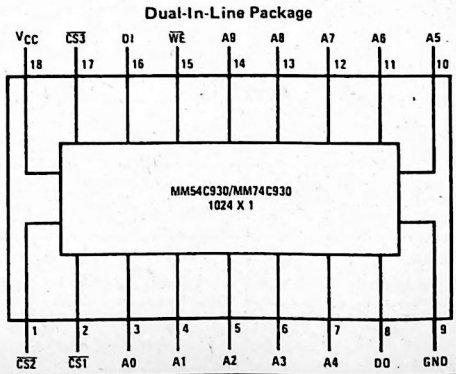


FIGURE 1. Block Diagram





MOS EPROMs

MM1702A 2048-bit electrically programmable ROM

general description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

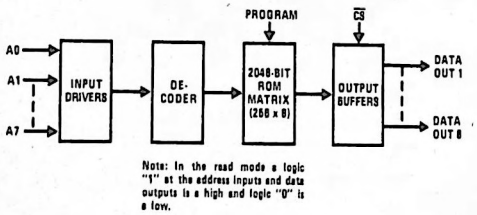
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

features

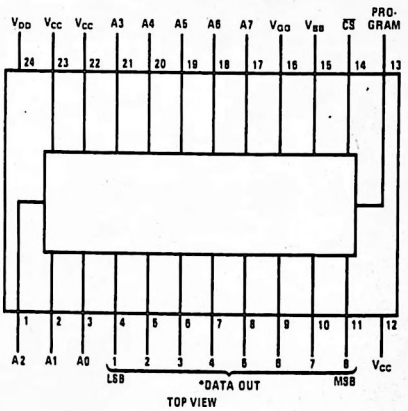
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AD
See Package 6
Order Number MM1702AQ
See Package 21

Pin Names

A0—A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1—8 are pins 4—11 respectively.

JULY 1976

MM1742 2048-bit read only memory

general description

The MM1742 is a 2048-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 256 8-bit words. Programming of the memory is accomplished by storing a charge in a cell location by applying a −47V pulse. Although a PROM die is used, factory programming is required.

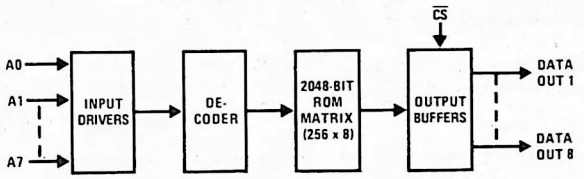
features

- Electrically programmed for fast turn-around
- Fully decoded, 256 x 8 organization
- Bipolar compatible
- TRI-STATE® outputs
- Pin compatible with the MM1702A, C1702A, and C1302.

applications

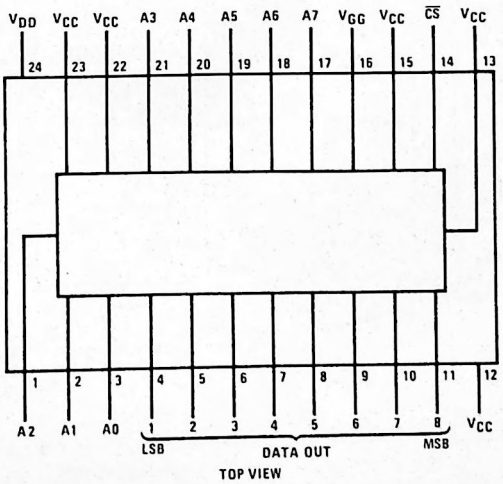
- Code conversion
- Table look-up
- Micro-programming
- Character generator
- Random logic synthesis

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT1} - D_{OUT8}$	Data Outputs

MARCH 1977

MM2708, MM2704 8k and 4k UV Erasable PROM

General Description

The MM2708, MM2704 are high speed 8192/4096-bit UV erasable and electrically reprogrammable EPROMs ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

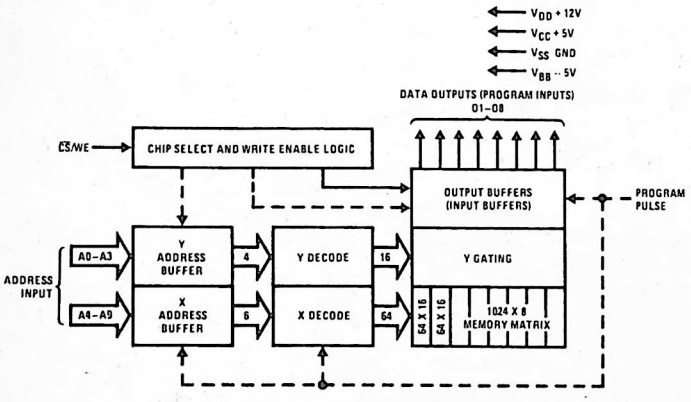
The MM2708, MM2704 are packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices by following the programming procedure.

The MM2708, MM2704 is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

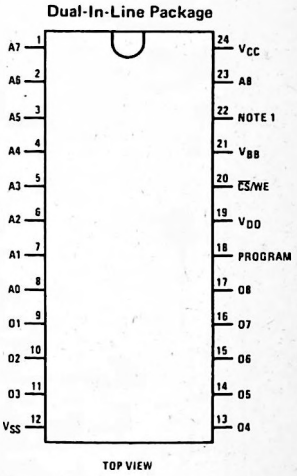
Features

- 1024 x 8 organization (MM2708)
- 512 x 8 organization (MM2704)
- 800 mW max
- Low power during programming
- Access time—450 ns max
- Standard power supplies: 12V, 5V, −5V
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams



Dual-In-Line Package



Note. MM2704: Pin 22 = V_{SS}
MM2708: Pin 22 = A9

Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
CS/WE	Chip select/write enable input

MOS EPROMs

MM4203/MM5203 electrically programmable 2048-bit read only memory (pROM)

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

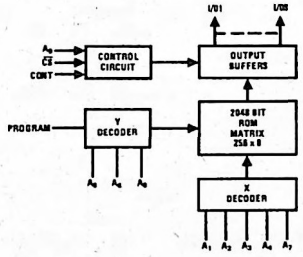
features

- Field programmable
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

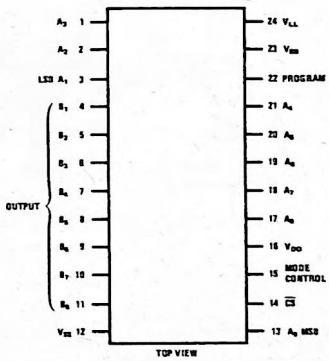
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



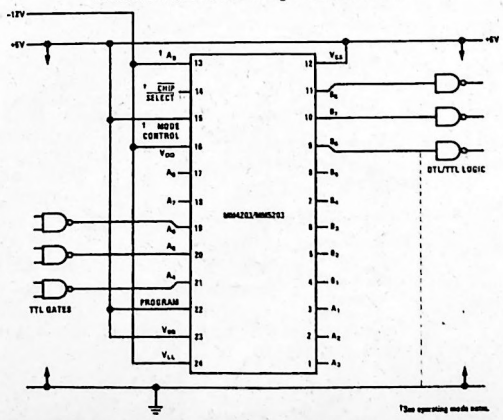
Dual-In-Line Package



Order Number MM4203D or MM5203D
See Package 6
Order Number MM4203Q or MM5203Q
See Package 21

typical applications

256 x 8 PROM Showing TTL Interface



Note: For programming information see AN-100.

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A_9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A_9 — Logic HIGH enables the odd (B_1, B_3..B_7) outputs
— Logic LOW enables the even (B_2, B_4.. B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

MM4243/MM5243 2048-bit read only memory

general description

The MM4243/MM5243 is a 2048-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 256 8-bit words or 512 4-bit words. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. Although a PROM die is used, factory programming is required. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

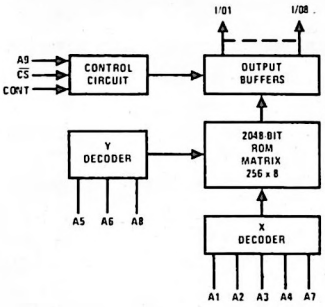
features

- Electrically programmed for fast turn-around
- Bipolar compatibility +5V, −12V operation
- High speed operation 1μs max access time
- Pin compatible with MM5203Q, EPROM and the MM5213 masked ROM
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- Chip select output control
- 256 x 8 or 512 x 4 organization

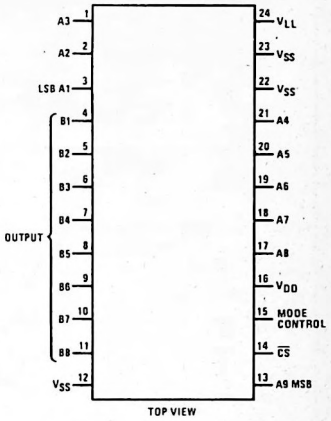
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



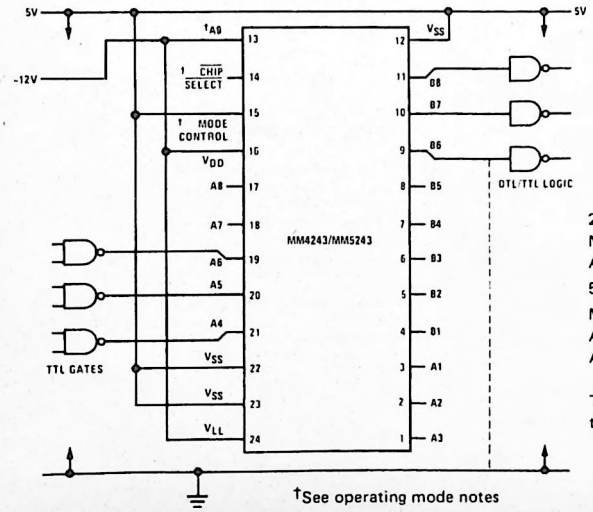
Dual-In-Line Package



TOP VIEW

typical application

256 x 8 PROM Showing TTL Interface



†See operating mode notes

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A9 — Logic HIGH enables the odd (B1, B3. . .B7) outputs
A9 — Logic LOW enables the even (B2, B4. . .B8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

MOS EPROMs

MM4204/MM5204
electrically programmable 4096-bit read only memory (EROM)

general description

The MM4204/MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatiblity. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications

features

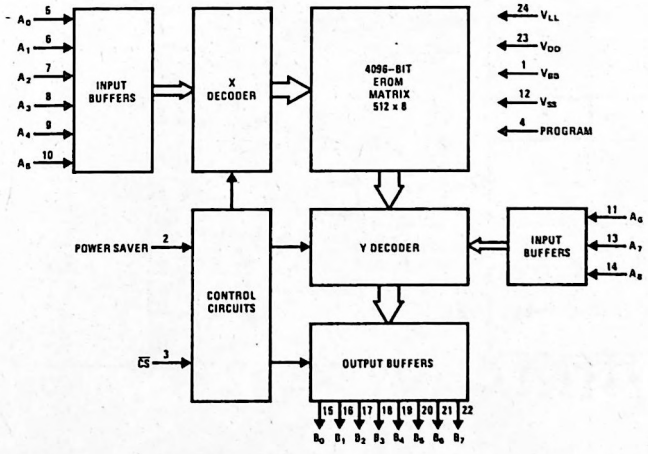
- Field programmable
- Fast program time: ten seconds typical for 4096-bits
- Fast access time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL compatibility

applications

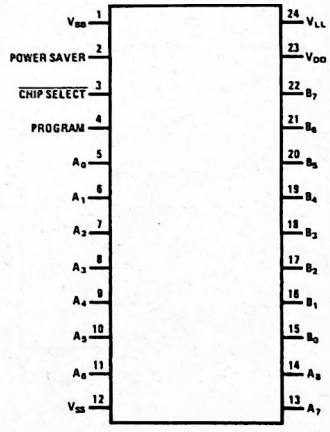
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

4

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D or MM5204D
See Package 6

Order Number MM4204Q or MM5204Q
See Package 21

MM4244/MM5244 4096-bit read only memory

general description

The MM4244/MM5244 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. Although a PROM die is used, factory programming is required. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

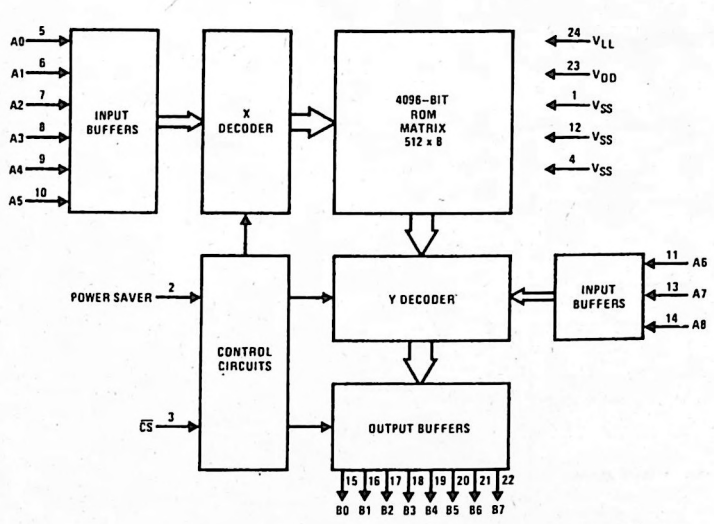
features

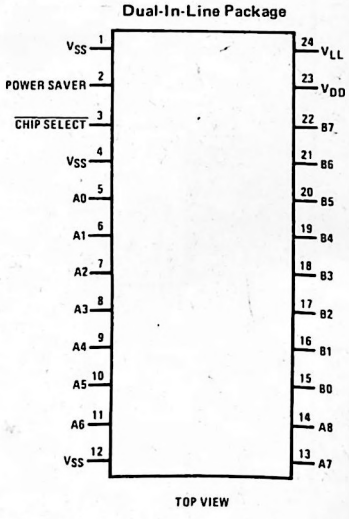
- Electrically programmed for fast turn-around
- Fast access time
  - MM4244 1.25μs
  - MM5244 1μs
- DTL/TTL compatibility
- Pin compatible with the MM5204 and the MM5214
- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- Low power dissipation
- "Power Saver" control for low power applications

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams

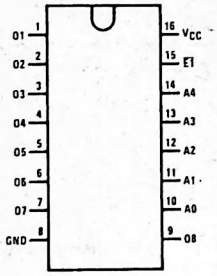




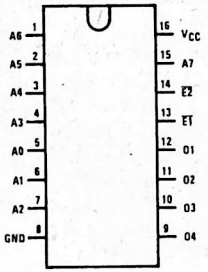
NATIONAL SEMICONDUCTOR BIPOLAR PROM/ROM SELECTION GUIDE

JANUARY 1977

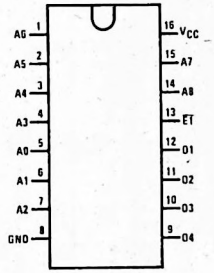
CONNECTION DIAGRAMS (Top Views)



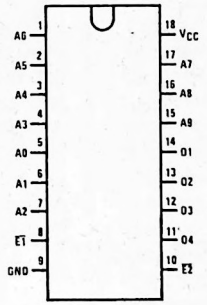
DM7577, DM8577,
DM7578, DM8578



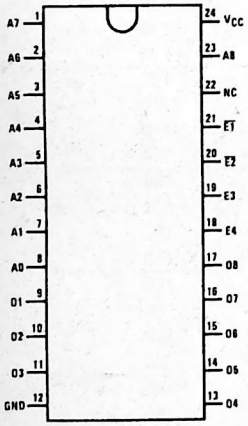
DM54S387, DM74S387,
DM54S287, DM74S287



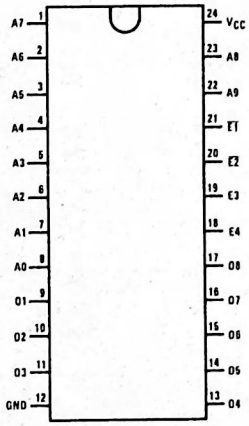
DM54S570, DM74S570,
DM54S571, DM74S571



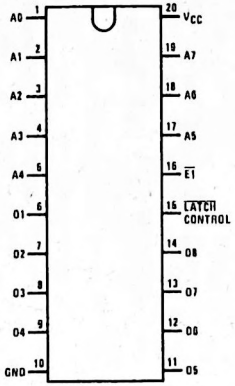
DM54S572, DM74S572,
DM54S573, DM74S573



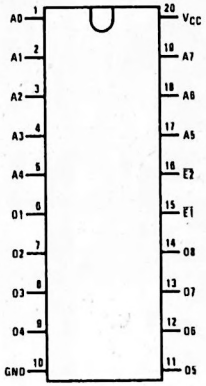
DM77S295, DM87S295,
DM77S296, DM87S296



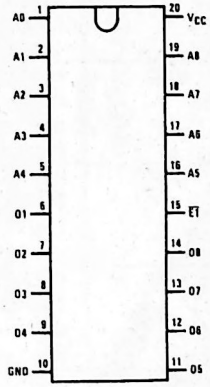
DM77S229, DM87S229,
DM77S228, DM87S228



DM77S221, DM87S221,
DM77S222, DM87S222



DM54S470, DM74S470,
DM54S471, DM74S471



DM54S473, DM74S473,
DM54S472, DM74S472

NATIONAL SEMICONDUCTOR BIPOLAR PROM/ROM SELECTION GUIDE

JANUARY 1977

TOTAL BITS	PART NUMBER		ORGANIZATION	NUMBER OF PINS	TEMPERATURE RANGE	MAXIMUM ADDRESS ACCESS (t_{AA})	MAXIMUM SUPPLY CURRENT (I_{CC})
	PROM	ROM					
256	DM7577	DM5488	32 x 8 OC	16	−55°C to +125°C	70	110
	DM8577	DM7488	32 x 8 OC	16	0°C to +70°C	50	110
	DM7578	DM7598	32 x 8 TS	16	−55°C to +125°C	70	110
	DM8578	DM8598	32 x 8 TS	16	0°C to +70°C	50	110
1024	DM54S387	DM54S187	256 x 4 OC	16	−55°C to +125°C	60	130
	DM74S387	DM74S187	256 x 4 OC	16	0°C to +70°C	50	130
	DM54S287	DM75S97	256 x 4 TS	16	−55°C to +125°C	60	130
	DM74S287	DM85S97	256 x 4 TS	16	0°C to +70°C	50	130
2048	DM54S570	DM54S270	512 x 4 OC	16	−55°C to +125°C	70	130
	DM74S570	DM74S270	512 x 4 OC	16	0°C to +70°C	55	130
	DM54S571	DM54S370	512 x 4 TS	16	−55°C to +125°C	70	130
	DM74S571	DM74S370	512 x 4 TS	16	0°C to +70°C	55	130
4096	DM54S572		1k x 4 OC	18	−55°C to +125°C	75	140
	DM74S572		1k x 4 OC	18	0°C to +70°C	60	140
	DM54S573		1k x 4 TS	18	−55°C to +125°C	75	140
	DM74S573		1k x 4 TS	18	0°C to +70°C	60	140
4096	DM77S295	DM77S95	512 x 8 OC	24	−55°C to +125°C	80	170
	DM87S295	DM87S95	512 x 8 OC	24	0°C to +70°C	65	170
	DM77S296	DM77S96	512 x 8 TS	24	−55°C to +125°C	80	170
	DM87S296	DM87S96	512 x 8 TS	24	0°C to +70°C	65	170
8192	DM77S229	DM75S29	1k x 8 OC	24	−55°C to +125°C	90	170
	DM87S229	DM85S29	1k x 8 OC	24	0°C to +70°C	70	170
	DM77S228	DM75S28	1k x 8 TS	24	−55°C to +125°C	90	170
	DM87S228	DM85S28	1k x 8 TS	24	0°C to +70°C	70	170
2048	DM77S221	DM77S201	256 x 8 OC	20	−55°C to +125°C	75	150
	DM87S221	DM87S201	256 x 8 OC	20	0°C to +70°C	60	150
	DM77S222	DM77S202	256 x 8 TS	20	−55°C to +125°C	75	150
	DM87S222	DM87S202	256 x 8 TS	20	0°C to +70°C	60	150
2048	DM54S470	DM54S271	256 x 8 OC	20	−55°C to +125°C	75	150
	DM74S470	DM74S271	256 x 8 OC	20	0°C to +70°C	60	150
	DM54S471	DM54S371	256 x 8 TS	20	−55°C to +125°C	75	150
	DM74S471	DM74S371	256 x 8 TS	20	0°C to +70°C	60	150
4096	DM54S473		512 x 8 OC	20	−55°C to +125°C	80	165
	DM74S473		512 x 8 OC	20	0°C to +70°C	65	165
	DM54S472		512 x 8 TS	20	−55°C to +125°C	80	165
	DM74S472		512 x 8 TS	20	0°C to +70°C	65	165

National Semiconductor

Bipolar PROMs

PRELIMINARY

DM54S188/DM74S188 open-collector 256-bit PROM
DM54S288/DM74S288 TRI-STATE® 256-bit PROM

general description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as ROM's as well as PROM's.

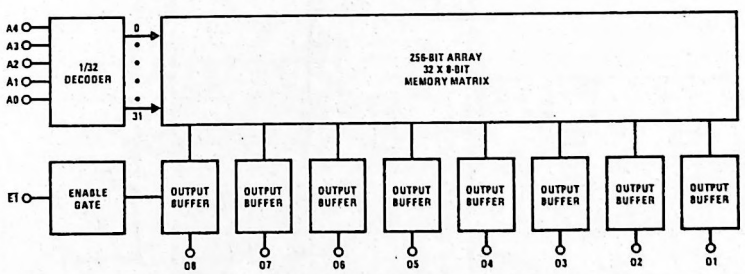
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—30 ns max
  - Enable access—20 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming

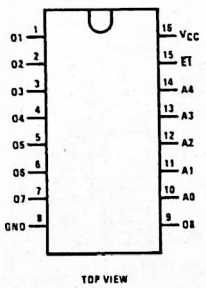
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J
DM74S288		X		X	N, J
DM54S188	X		X		J
DM54S288	X			X	J

block diagram



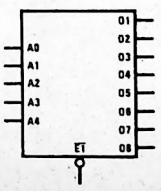
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



JULY 1976

DM54S287/DM74S287 TRI-STATE® 1024-bit PROM
DM54S387/DM74S387 open-collector 1024-bit PROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

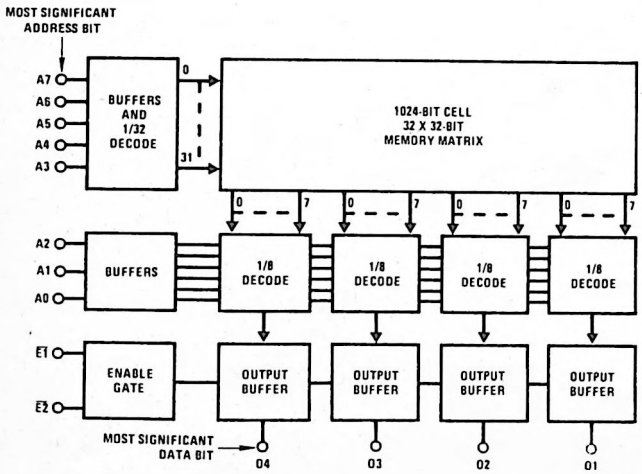
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—50 ns max
  Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S187 and DM85S97

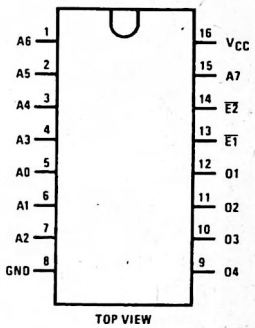
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J
DM74S287		X		X	N, J
DM54S387	X		X		J
DM54S287	X			X	J

block diagram



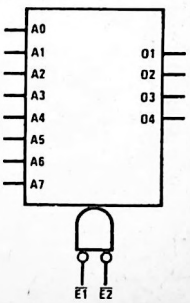
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



National Semiconductor

Bipolar PROMs

DM54S470/DM74S470 open-collector 2048-bit PROM
DM54S471/DM74S471 TRI-STATE® 2048-bit PROM

general description

These Schottky PROM memories are organized in the popular 256 words by 8 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

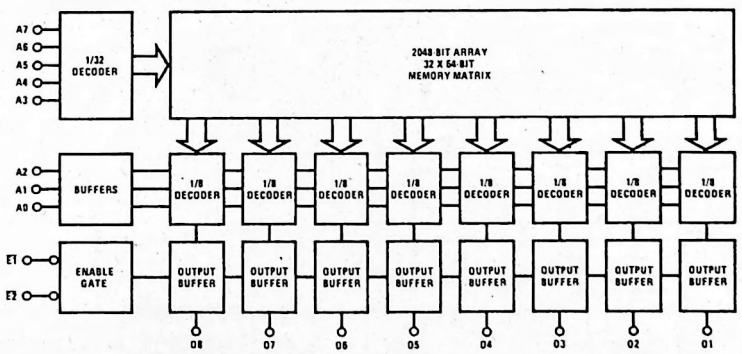
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- High density 20-pin package
- ROM mates are DM74S271 and DM74S371

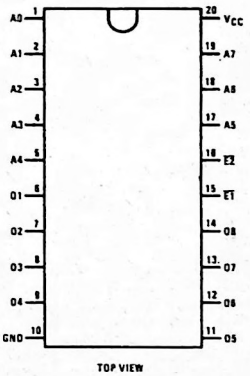
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S470		X	X		N, J
DM74S471		X		X	N, J
DM54S470	X		X		J
DM54S471	X			X	J

block diagram



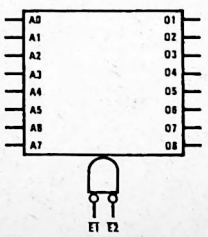
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Preliminary

DM54S473/DM74S473 open-collector 4096-bit PROM
DM54S472/DM74S472 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions.

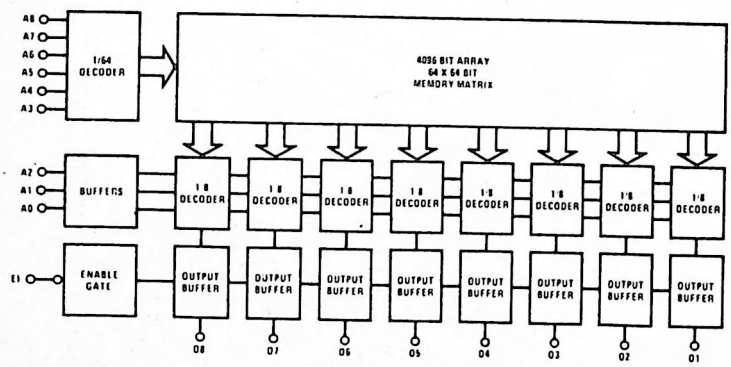
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—65 ns max
  - Enable access—40 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 20-pin package

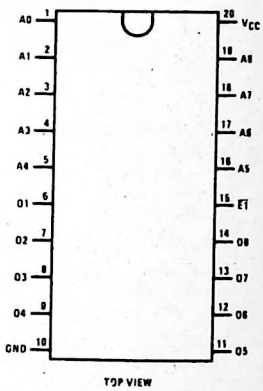
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N, J
DM74S472		X		X	N, J
DM54S473	X		X		J
DM54S472	X			X	J

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol

National Semiconductor

Bipolar PROMs

DM54S570/DM74S570 open-collector 2048-bit PROM
DM54S571/DM74S571 TRI-STATE® 2048-bit PROM

general description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

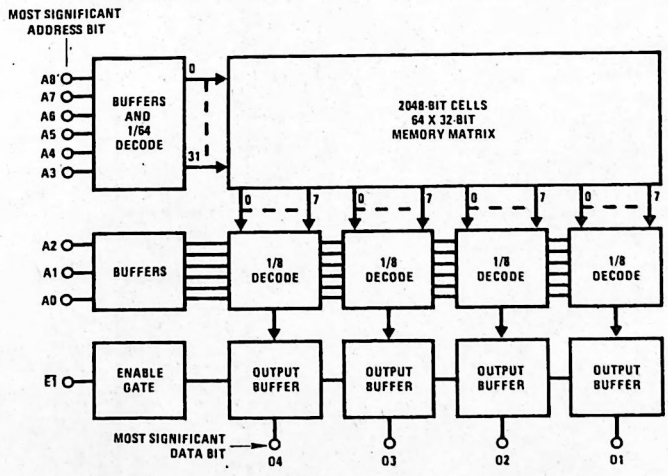
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

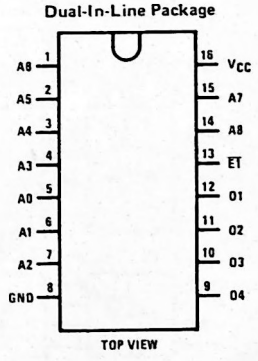
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

block diagram

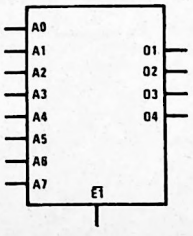


connection diagram

Dual-In-Line Package



logic symbol



5

Preliminary

DM54S572/DM74S572 open-collector 4096-bit PROM
DM54S573/DM74S573 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

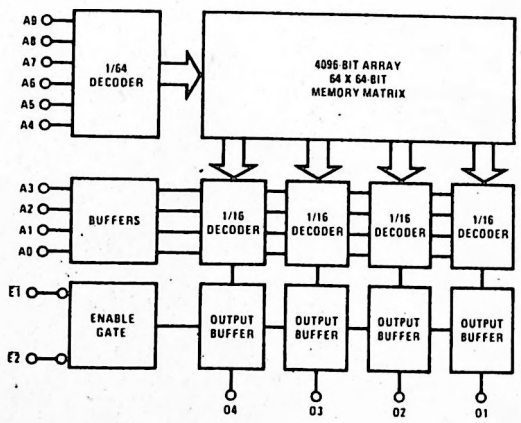
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—60 ns max
  - Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

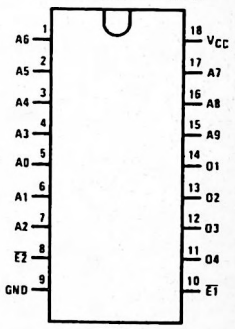
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N, J
DM74S573		X		X	N, J
DM54S572	X		X		J
DM54S573	X			X	J

block diagram



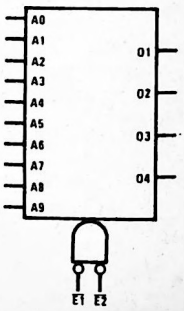
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Bipolar PROMs

DM7577/DM8577 256-bit programmable read only memory

general description

The DM7577/DM8577 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The organization is expandable to 1,856 words of n-bits with no additional output buffering.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7577/DM8577 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7577/DM8577 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

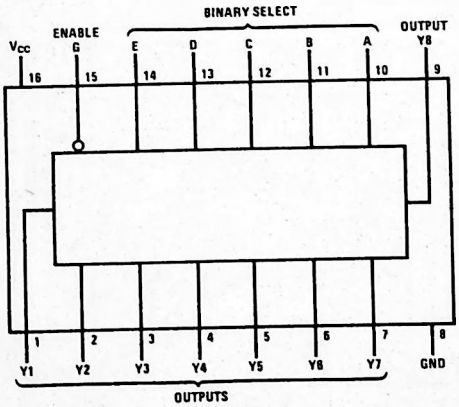
The mask-programmable DM5488/DM7488 can be used to replace the DM7577/DM8577 as they are functionally and mechanically identical.

features

- Field programmable for custom or prototype memories
- Mask-programmable DM5488/DM7488 is a direct replacement for the DM7577/DM8577
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- Open-collector outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM7577D
or DM8577D
See Package 3

Order Number DM8577N
See Package 15

DM7578/DM8578 TRI-STATE® 256-bit programmable read only memory

general description

The DM7578/DM8578 is a field-programmable, 256-bit, read only memory organized as 32 words of 8 bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain in the high impedance (Z) state.

The address of an 8-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple DM7578/DM8578 devices are used in a memory system, the enable input allows easy decoding of additional address bits. The TRI-STATE outputs eliminates the need for external pull-up resistors, and provides good capacitance drive capability.

Data can be electronically programmed, as desired, at any of the 256-bit locations of the DM7578/DM8578 in accordance with the programming procedure specified. Prior to programming, the memory contains a high-logic-level output condition at all 256 bit locations. The programming procedure open-circuits nichrome links which results in a low-logic-level output at selected locations.

The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a low logic level. Outputs never having been altered may later be programmed to supply a low-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

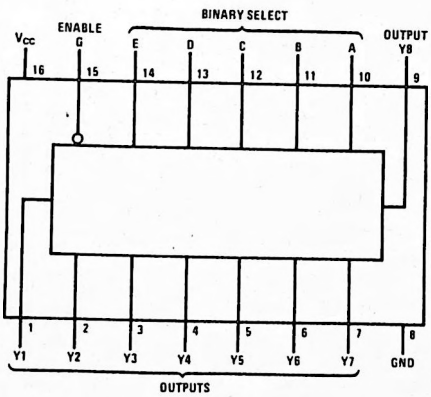
The mask-programmable DM7598/DM8598 can be used to replace the DM7578/DM8578 as they are functionally and mechanically identical.

features

- Field programmable for custom or prototype memories
- Mask-programmable DM7598/DM8598 is a direct replacement for the DM7578/DM8578.
- Typical access time 35 ns
- Organized as 32 words of 8-bits each
- Ideal for microprogramming and code converters
- TRI-STATE outputs are easily expanded
- Fully-decoded buffered inputs
- Fully compatible with most TTL and DTL circuits
- Pin compatible with SN74188A

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM7578D or DM8578D
See Package 3
Order Number DM8578N
See Package 15

Preliminary

DM77S221/DM87S221 open-collector 2048-bit PROM with latches
DM77S222/DM87S222 TRI-STATE® 2048-bit PROM with latches

general description

These Schottky PROM memories are organized in the popular 256 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word. An output latch control is provided. If the latch control pin is high, the data falls through to the output enable gate. If the latch control pin is low, the data is latched and the addresses may be changed without affecting the output data.

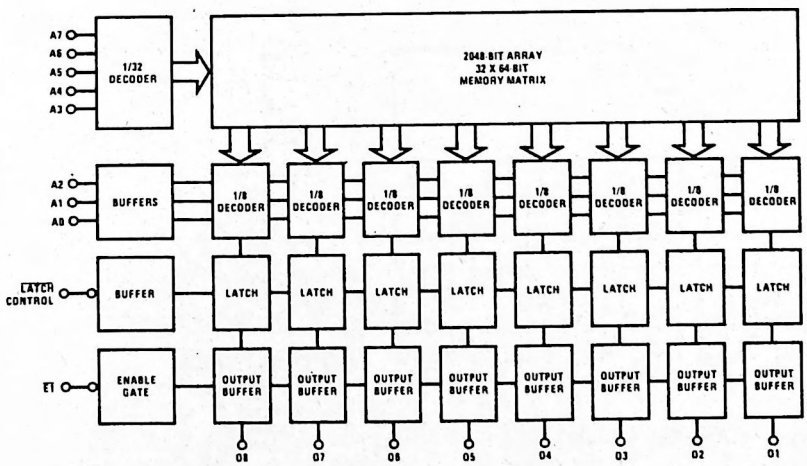
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

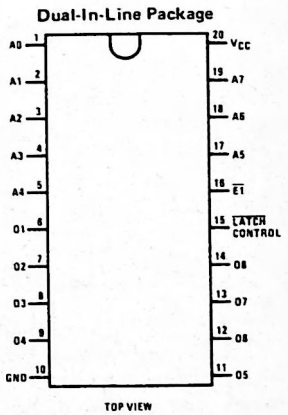
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—60 ns max
  - Enable access— 30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector or TRI-STATE® outputs
- Board level programming
- High density 20-pin package
- ROM mates are DM87S201 and DM87S202

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S221		X	X		N, J
DM87S222		X		X	N, J
DM77S221	X		X		J
DM77S222	X			X	J

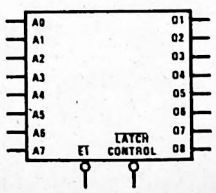
block diagram



connection diagram



logic symbol



5

Preliminary

DM77S229/DM87S229 open-collector 8196-bit PROM
DM77S228/DM87S228 TRI-STATE® 8196-bit PROM

general description

These Schottky PROM memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

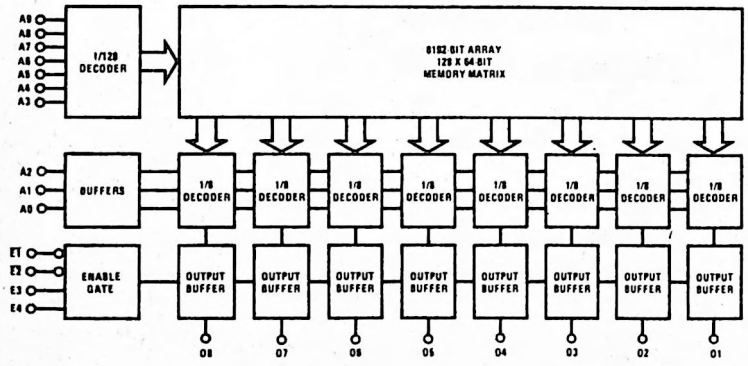
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—70 ns max
  Enable access—45 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM85S29 and DM85S28

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S229		X	X		N, J
DM87S228		X		X	N, J
DM77S229	X		X		J
DM77S228	X			X	J

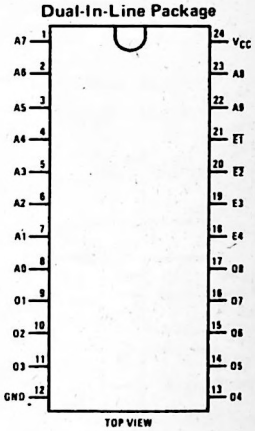
block diagram



The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

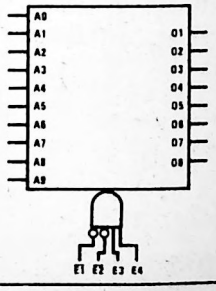
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



DM77S295/DM87S295 open-collector 4096-bit PROM
DM77S296/DM87S296 TRI-STATE® 4096-bit PROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

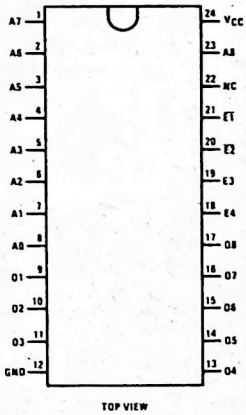
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

selection guide

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S295		X	X		N, J
DM87S296		X		X	N, J
DM77S295	X		X		J
DM77S296	X			X	J

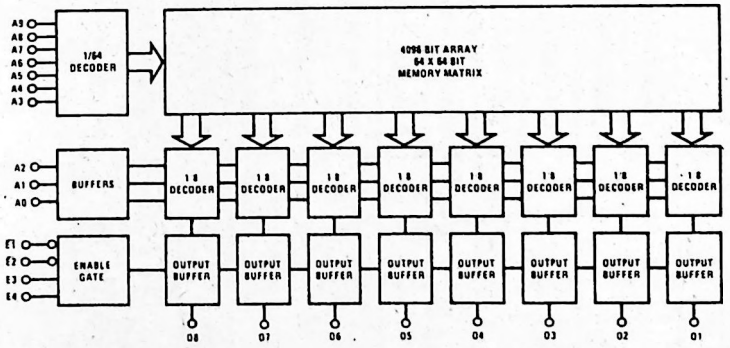
connection diagram

Dual-In-Line Package



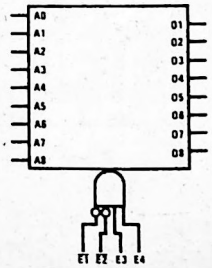
TOP VIEW

block diagram



The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

logic symbol



5

NATIONAL SEMICONDUCTOR BIPOLAR PROM CROSS REFERENCE GUIDE

MARCH 1977

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	FAIRCHILD M = MIL C = COM	HARRIS 2 = MIL 5 = COM	INTEL M = MIL P = COM	INTERSIL M = MIL C = COM	M.M.I. MIL/COM –1 = SCHOTTKY	SIGNETICS S = MIL N = COM	T.I. MIL/COM
256-Bit (32 x 8) 16-Pin	OC	DM7577/DM8577	AM27S08		HM1-7602 HM1-8256		IM5600	5330/6330	8223 82S23	SN54188A/74188A SN54S188/74S188
	TS	DM7578/DM8578	AM27S09		HM1-7603		IM5610	5331/6331	82S123	SN54S288/74S288
1024-Bit (256 x 4) 16-Pin	OC	DM54S387/DM74S387	AM27S10	93417 93416	HM1-7610 HM1-1024A	3601-1 3601	IM5603	5300/6300	82S126	SN54S387/74S387
	TS	DM54S287/DM74S287	AM27S11	93427 93426	HM1-7611 HM1-1024	3621	IM5623	5301/6301	82S129	SN54S287/74S287
2048-Bit (512 x 4) 16-Pin	OC	DM54S570/DM74S570		93436	HM1-7620	3602	IM5604	5305/6305	82S130	
	TS	DM54S571/DM74S571		93446	HM1-7621	3622	IM5624	5306/6306	82S131	
4096-Bit (512 x 8) 24-Pin	OC	DM77S295/DM87S295		93438	HM1-7640	3604	IM5605	5340/6340	82S140	SN54S474/74S474
	TS	DM77S296/DM87S296		93448	HM1-7641	3624	IM5625	5341/6341	82S141	SN54S475/74S475
2048-Bit (256 x 8) 20-Pin	OC	DM54S470/DM74S470						5308/6308		SN54S470/74S470
	TS	DM54S471/DM74S471						5309/6309		SN54S471/74S471
4096-Bit (512 x 8) 20-Pin	OC	DM54S473/DM74S473						5348/6348		SN54S473/74S473
	TS	DM54S472/DM74S472						5349/6349		SN54S472/74S472
4096-Bit (1024 x 4) 18-Pin	OC	DM54S572/DM74S572*		93452	HM1-7642	3605	IM5606	5352/6352	82S136	
	TS	DM54S573/DM74S573*		93453	HM1-7643	3625	IM5626	5353/6353	82S137	
8192-Bit (1024 x 8) 24-Pin	OC	DM77S229/DM87S229*				3608	IM5608	5380/6380	82S180	
	TS	DM77S228/DM87S228*				3628	IM5618	5381/6381	82S181	
8192-Bit (2048 x 4) 18-Pin	OC	DM54S672/DM74S672*					IM56S01		82S184	
	TS	DM54S673/DM74S673*					IM56S11		82S185	

Note: All manufacturer's PROMs program differently.

*Future products

National Semiconductor

PROM programming procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

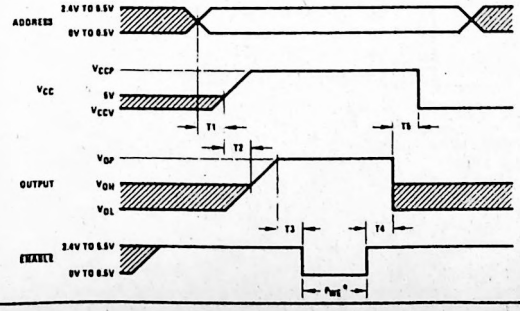
1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when V_{CC} is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to one or both enable inputs.
   b) Increase V_{CC} to 10.5V ±0.5V with the rate of increase being between 1.0 and 10.0V/μs. Since V_{CC} supplies the current to program the fuse as well as the I_{CC} of the device at programming voltage, it must be capable of supplying 400 mA at 11.0V.
   c) Select the output where a high level is desired by raising that output voltage to 10.5V ±0.5V. Limit the rate of increase to a value between 1.0 and 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC} but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 kΩ. (Remember that the outputs of the device are still disabled at this time because the chip enables are high.)
   d) Enable the device by taking both chip enables to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ±0.2V. Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device.

	PARAMETERS	CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC}=11V	600		750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT}=11V			20	mA
t_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms



T1 = 100 ns min
T2 = 5μs min (T2 may be ≥ 0 if V_{CCP} rises at the same rate or faster than V_{OP})
T3 = 100 ns min
T4 = 100 ns min
T5 = 100 ns min

*P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has programmed

National Semiconductor

MOS ROMs

MM2316A 16,384-bit read only memory

general description

The MM2316A is a static MOS 16,384-bit read-only memory organized in a 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

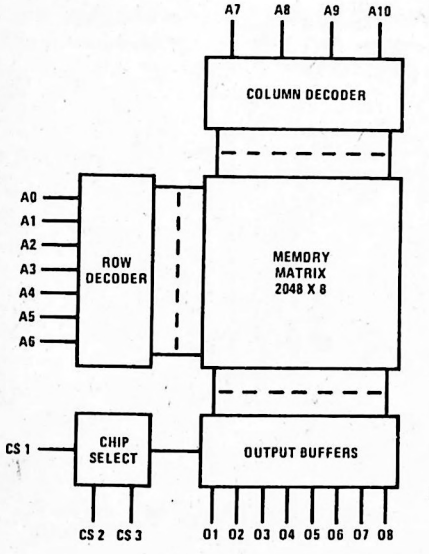
features

- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time—450 ns

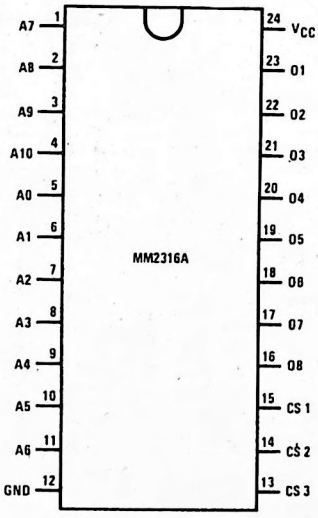
applications

- Microprogramming
- Control logic
- Table look-up

block and connection diagrams



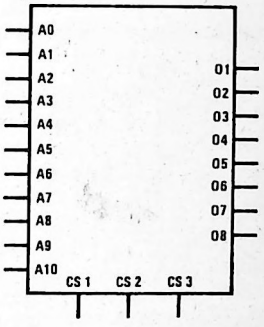
Dual-In-Line Package



TOP VIEW

Order Number MM2316AJ
See Package 11
Order Number MM2316AN
See Package 18A

logic symbol



Preliminary

MM2316 E 16,384-bit read only memory

general description

The MM2316E is a static MOS 16.348-bit read-only memory organized in a 2048-word-by-8-bit-format. It is fabricated using N-channel enhacement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and single power supply operation.

Three programmable chip selects controlling the TRI-STATE outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

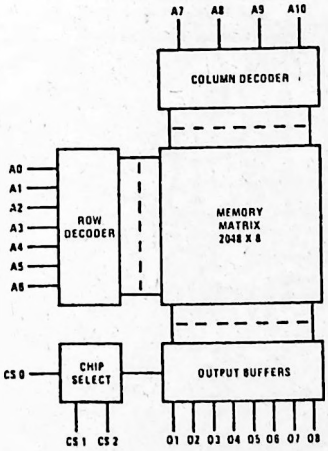
features

- EPROM/ROM Compatible for Cost-Effective System Development
- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time - 450ns

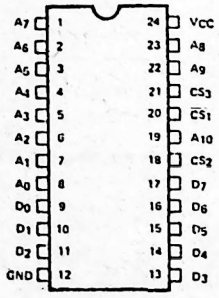
applications

- Microprogramming
- Control logic
- Table look-up

block and connection diagrams



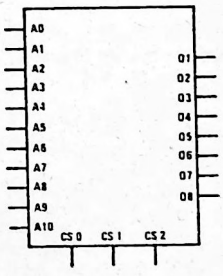
PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
D_7–D_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

logic symbol



6

MM3501 1024-bit read-only memory

general description

The MM3501 is a 1024-bit read-only memory programmed in a 128 word by 8 bit format. It is an MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory is specified by the customer and customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

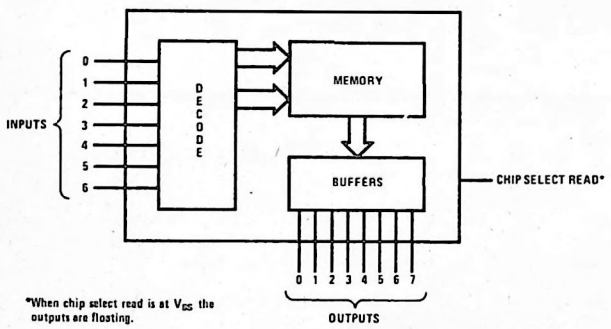
features

- Chip select
- 1.5 μs typical access time
- 115 mW typical static operation
- Low power consumption
- Bipolar compatible outputs

applications

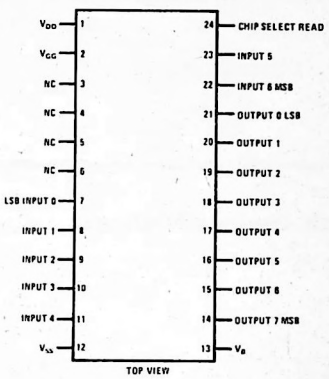
- Microprogramming
- Code conversion
- Table lookup
- Control logic

logic and connection diagrams



*When chip select read is at V_{GS} the outputs are floating.

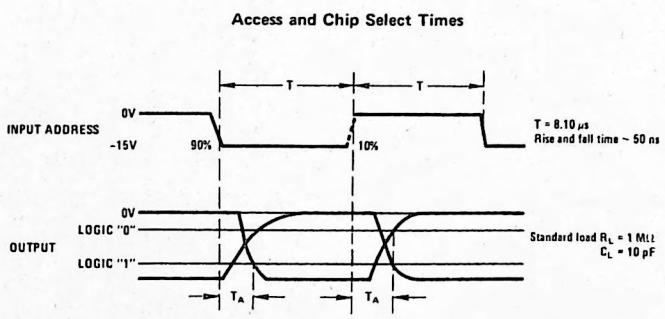
Dual-In-Line Package



Order Number MM3501J
See Package 11
Order Number MM3501N
See Package 18

switching time waveforms

Access and Chip Select Times



Note: The logic "0," "1" levels may be taken to be (−1.0V, −10V) or (−2.0V, −9.0V) respectively. Guaranteed limits are at −1.0V and −10V.

Note: For programming information see AN-100.

MOS ROMs

MM4210/MM5210 1024-bit read only memory

general description

The MM4210/MM5210 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

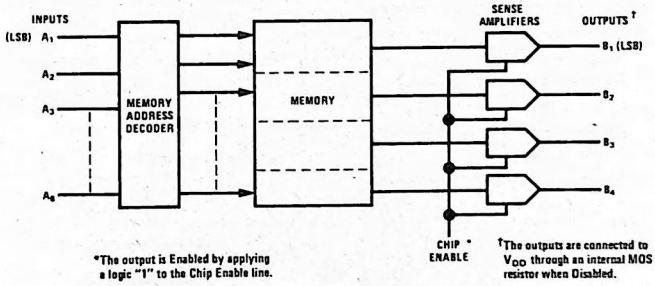
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

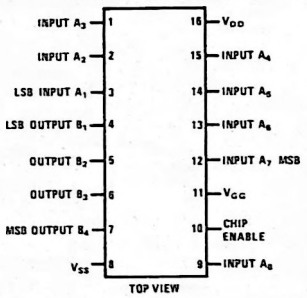
block and connection diagrams



*The output is Enabled by applying a logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

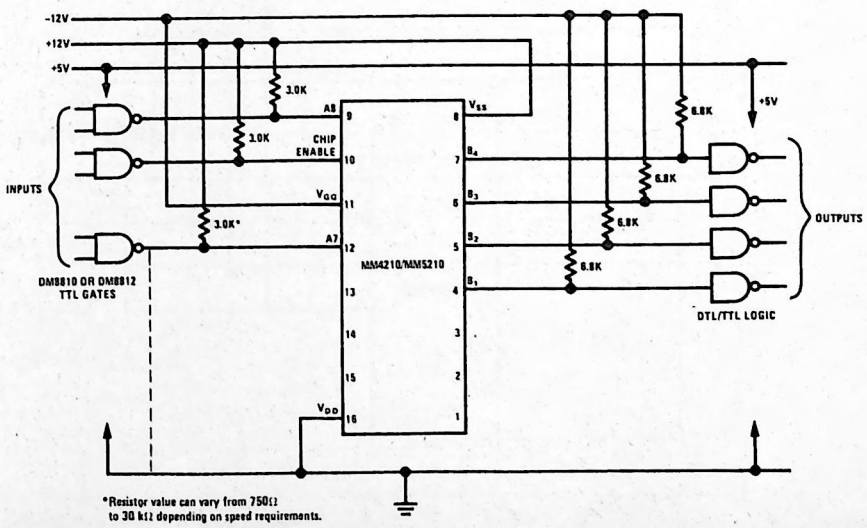
Dual-In-Line Package



Order Number MM4210J or MM5210J
See Package 10
Order Number MM5210N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



*Resistor value can vary from 750Ω to 30 kΩ depending on speed requirements.

Note: For programming information see AN-100.

MM4211/MM5211 1024-bit read only memory

general description

The MM4211/MM5211 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

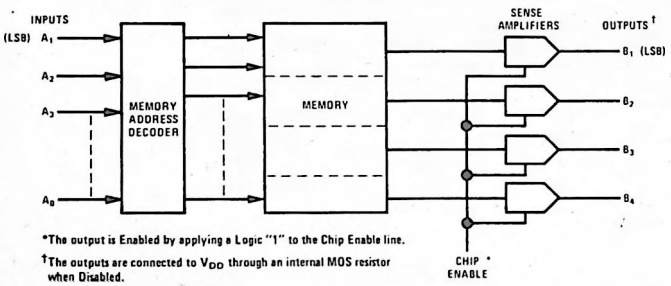
features

- Bipolar compatibility +5V, −12V operation
- High speed operation < 700 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

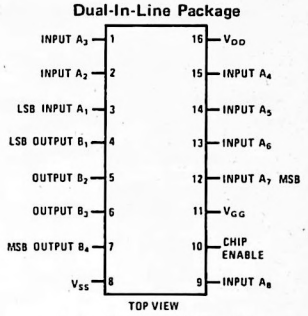
block and connection diagrams



*The output is Enabled by applying a Logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

Dual-In-Line Package

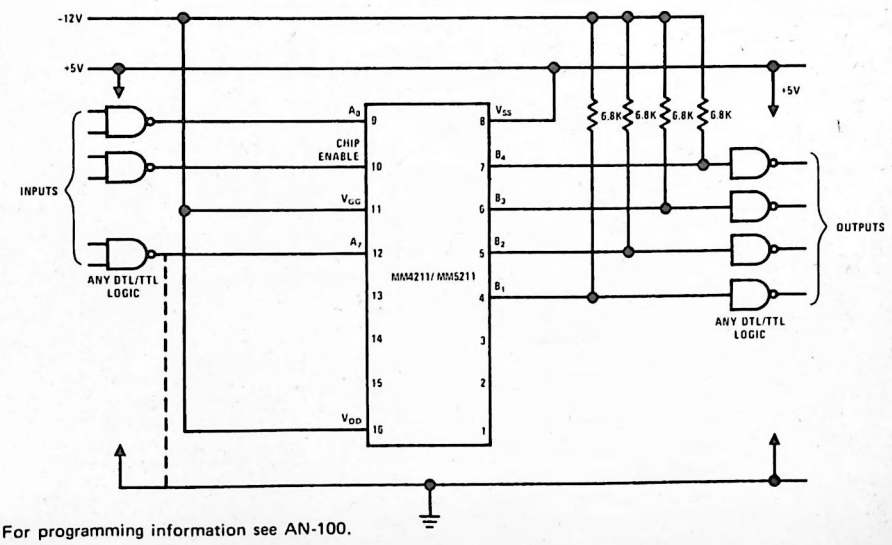


Order Number MM4211J or MM5211J
See Package 10

Order Number MM5211N
See Package 15

typical application

256 x 4 Bit ROM Showing TTL Interface



Note: For programming information see AN-100.

MOS ROMs

MM5212 12,288-bit read only memory

general description

The MM5212 12,288-bit read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology and ion-implanted resistors. Open drain outputs provide a TTL compatible wire OR capability with the addition of a 6.8 kΩ resistor. The ROM is organized in a 1024 word by 12-bit organization.

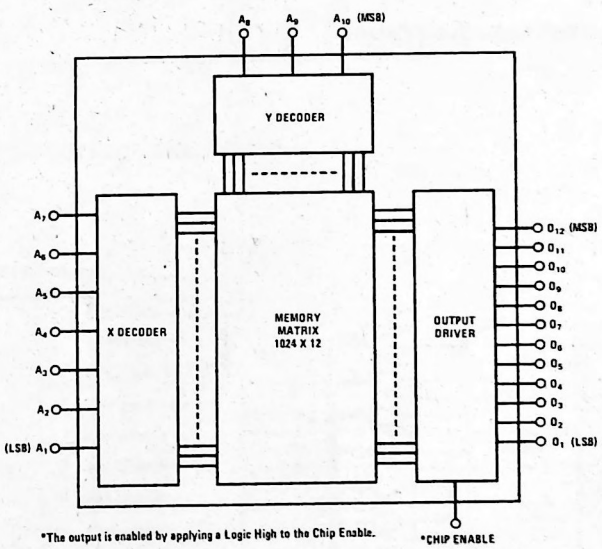
features

- Standard supplies +5.0V, −12V
- Open drain outputs Wire OR capability
- Static operation No clocks
- TTL compatible inputs and outputs

applications

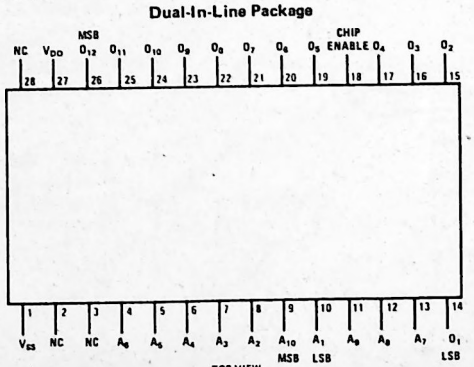
- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

schematic diagram



connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5212AD
See Package 7

Order Number MM5212AN
See Package 19

MOS ROMs

MM4213/MM5213 2048-bit read only memory

general description

The MM4213/MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

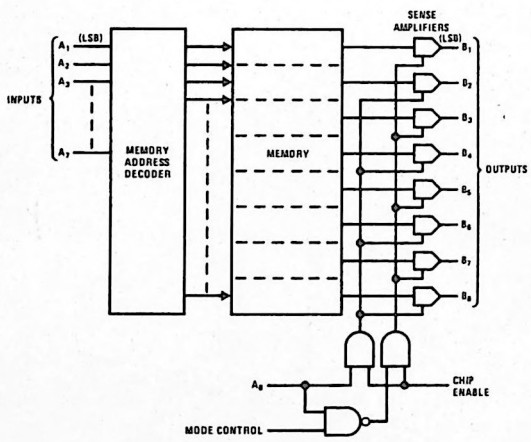
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 pROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

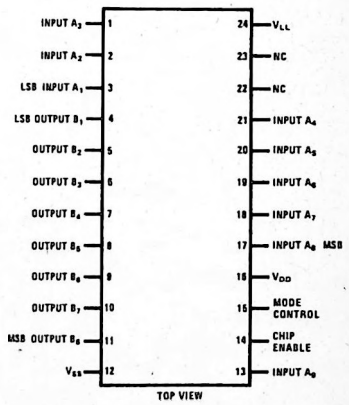
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4213J or MM5213J
See Package 11

Order Number MM5213N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4214/MM5214 4096-bit static read only memory

general description

The MM4214/MM5214 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

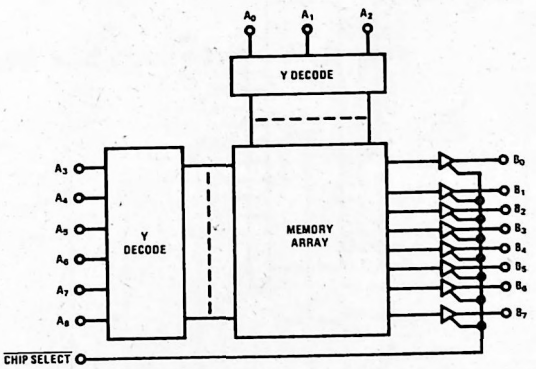
features

- Pin compatible with MM5204 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

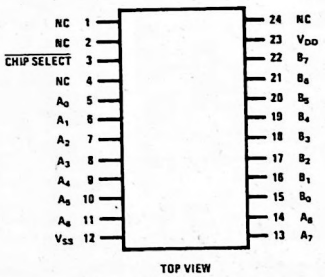
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package

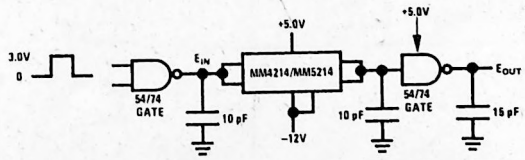


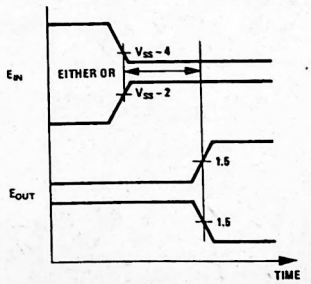
TOP VIEW

Order Number MM4214J or MM5214J
See Package 11

Order Number MM5214N
See Package 18

timing diagram/address time





Note: For programming information see AN-100.

MM5215 12,288-bit read only memory

general description

The MM5215 12,288-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology and ion-implanted resistors. TRI-STATE® outputs provide wire-OR capability without loading common data lines or reducing system access times. The ROM is organized in a 1024 x 12 bit word configuration. The V_{GG} supply may be brought to 0V to reduce internal power dissipation in the non-enabled mode to 10μW/bit.

Customer programs may be submitted on Hollerith coded punched cards.

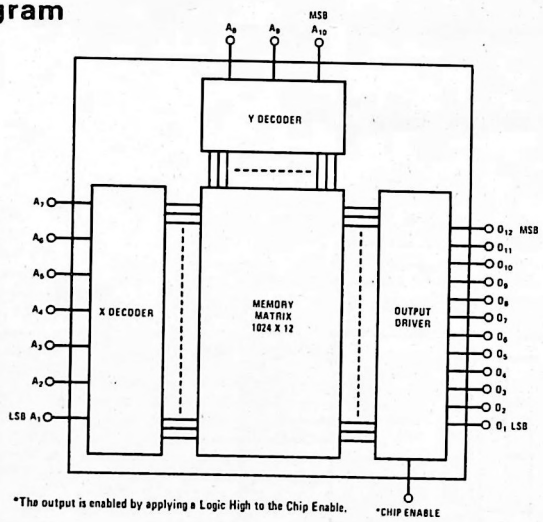
features

- Static operation
- TRI-STATE outputs
- No clocks required
- +12V and −12V supplies
- Pin compatible with E.A. 3800

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

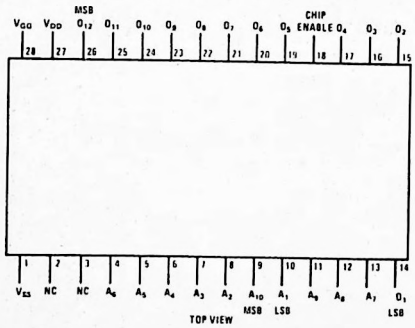
schematic diagram



*The output is enabled by applying a Logic High to the Chip Enable.

connection diagram

Dual-In-Line Package



Note: For programming information see AN-100.

Order Number MM5215AD
See Package 7

Order Number MM5215AN
See Package 19

MOS ROMs

MM4220/MM5220 1024-bit read only memory

general description

The MM4220/MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

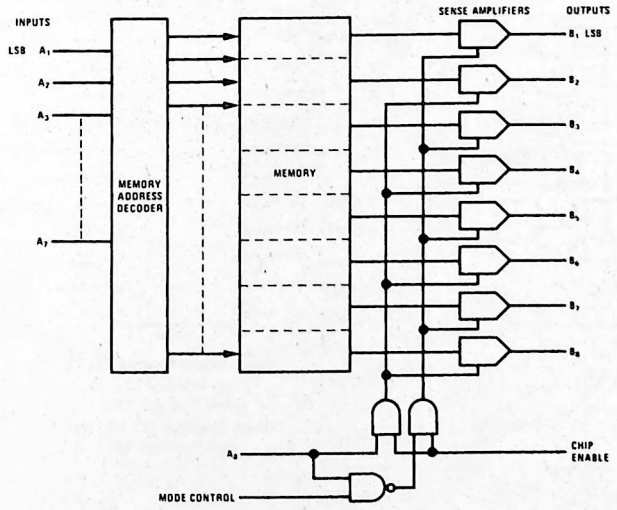
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

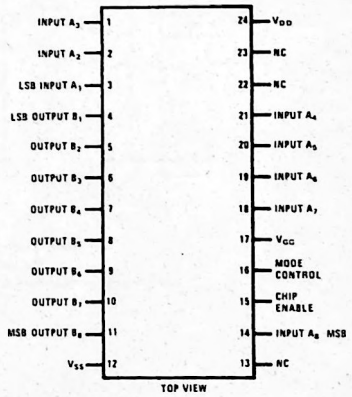
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

block and connection diagrams



Dual-In-Line Package



Order Number MM4220J
or MM5220J
See Package 11

Order Number MM5220N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4221/MM5221 1024-bit read only memory

general description

The MM4221/MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

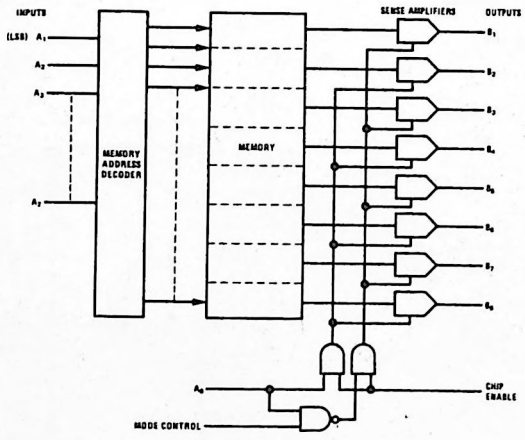
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — <700 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control

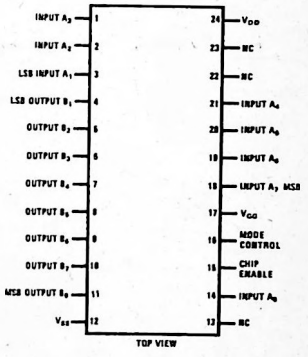
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4221J
or MM5221J
See Package 11
Order Number MM5221N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4229/MM5229 3072-bit read only memory (open drain)

general description

The MM4229/MM5229 is a 3072-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized in a 256 x 12 bit word configuration.

Customer programs may be supplied on Hollerith coded punched cards.

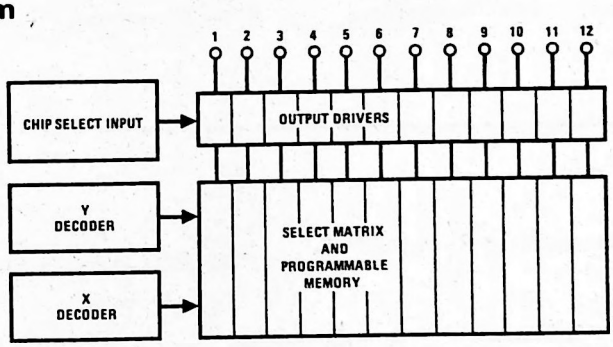
features

- TTL compatible
- Low standby power
- Programmable chip select inputs
- Typical 1.0μs access time
- Open drain outputs allow wire-OR of up to 8 devices

applications

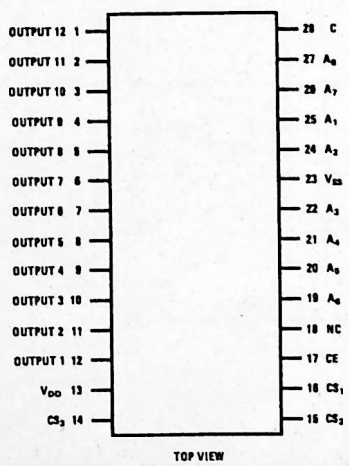
- Code conversion
- Random logic synthesis
- Table look-up
- Microprogramming

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Note: For programming information see AN-100.

Order Number MM4229D or MM5229D
See Package 7

Order Number MM5229N
See Package 19

MM4230/MM5230 2048-bit read only memory

general description

The MM4230/MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

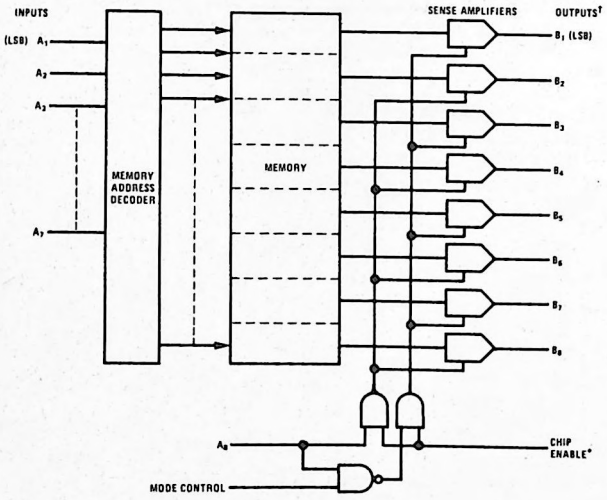
features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

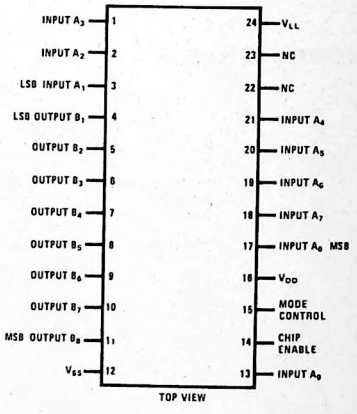
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

block and connection diagrams



Dual-In-Line Package



Order Number MM4230J
or MM5230J
See Package 11
Order Number MM5230N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4231/MM5231 2048-bit read only memory

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

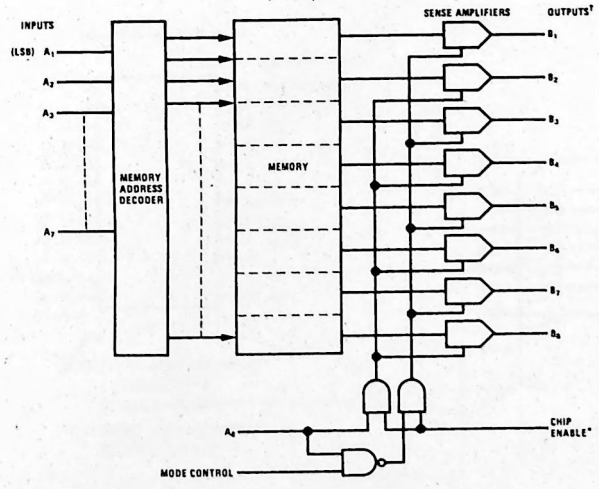
features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

applications

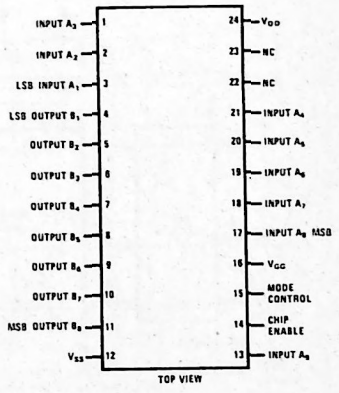
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

block and connection diagrams



† The outputs are open when Disabled.
* The output is enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



Order Number MM4231J
or MM5231J
See Package 11

Order Number MM5231N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4232/MM5232 4096-bit static read-only memory

general description

The MM4232/MM5232 4096-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

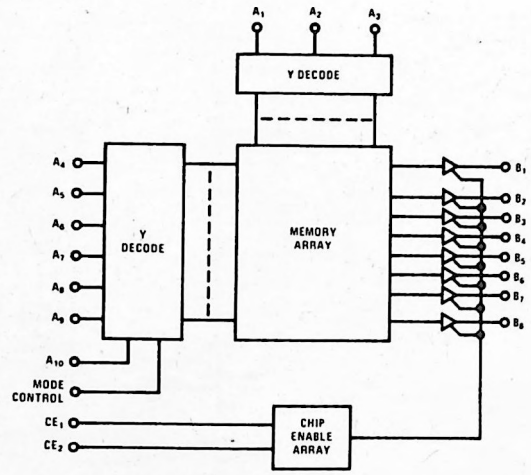
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

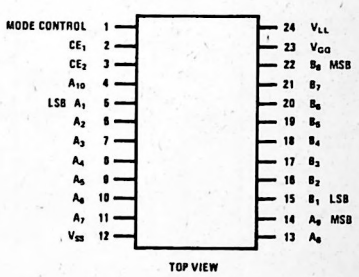
applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4232J or MM5232J
See Package 11
Order Number MM5232N
See Package 18

Note: For programming information see AN-100.

MOS ROMs

MM4233/MM5233 4096-bit read only memory

general description

The MM4233/MM5233 4096-bit static read only memory is a monolithic MOS integrated circuit utilizing P-channel ion-implanted enhancement mode low threshold technology to achieve bipolar compatibility. The ROM is organized in a 512 word x 8-bit format.

Four programmable chip selects provide logic control of the TRI-STATE® outputs, allowing wire OR capability of up to 16 ROM's without loading common data lines or reducing systems access times. A separate output supply lead V_{DD} is provided to reduce internal power dissipation in the output stages.

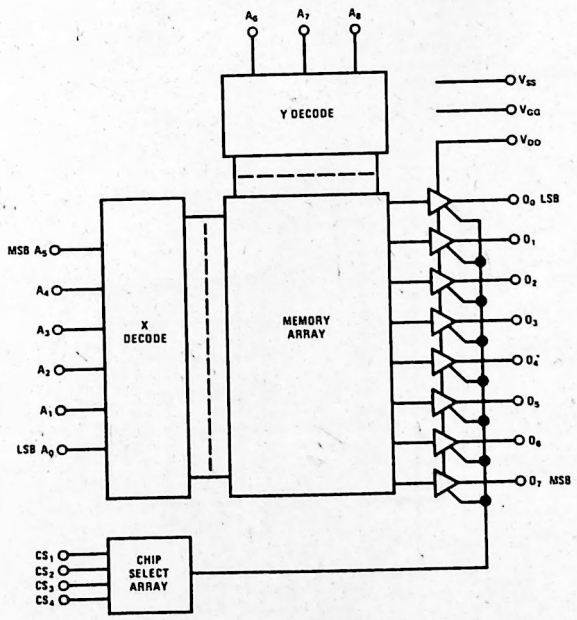
features

- Pin for pin compatible with the Fairchild 3514
- Bipolar compatible — No external components required
- Standard supplies — +5.0V, −12V
- TRI-STATE outputs — Bus ORable outputs
- Static operation — No clocks required
- Multiple ROM control — Four programmable chip select lines

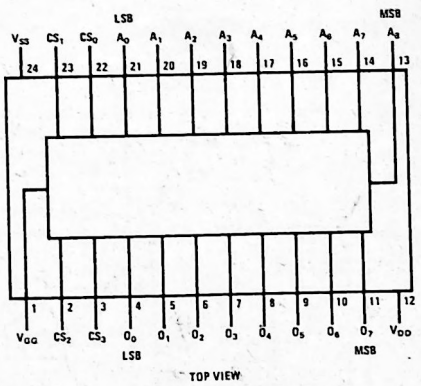
applications

- Code conversion
- Microprogramming
- Control logic
- Table look-up

logic and connection diagrams



Dual-In-Line Package



Order Number MM4233J or MM5233J
See Package 11

Order Number MM5233N
See Package 18

Note: For programming information see AN-100.

MM4240/MM5240 2560-bit static character generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64–8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

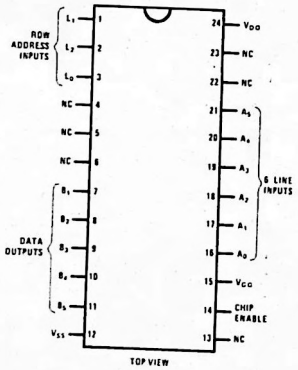
features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

applications

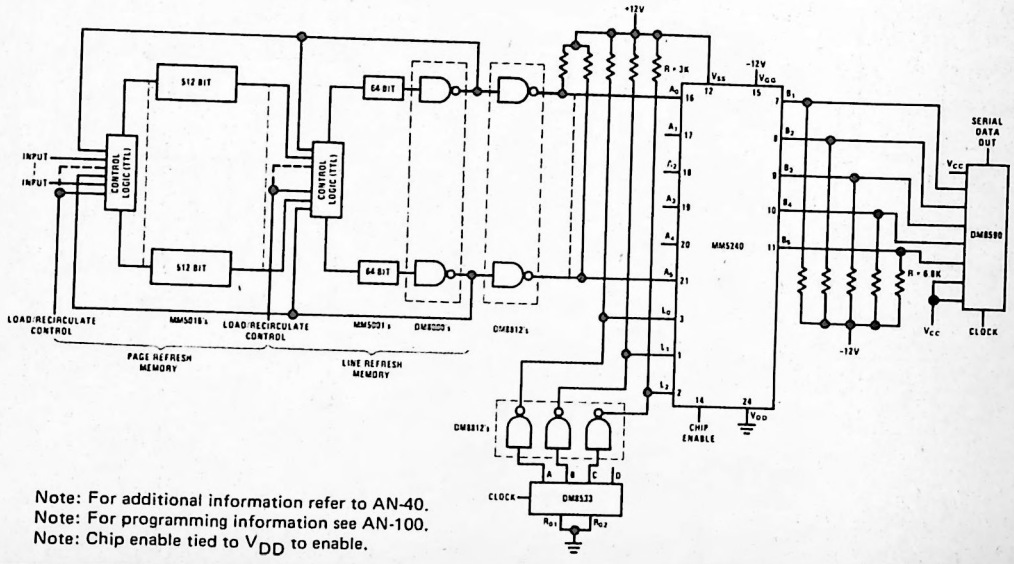
- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

connection diagram



Order Number MM4240J or MM5240J
See Package 11
Order Number MM5240N
See Package 18

typical application



Note: For additional information refer to AN-40.
Note: For programming information see AN-100.
Note: Chip enable tied to V_{DD} to enable.

MOS ROMs

MM4241/MM5241 3072-bit static read-only memory

general description

The MM4241/MM5241 3072-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

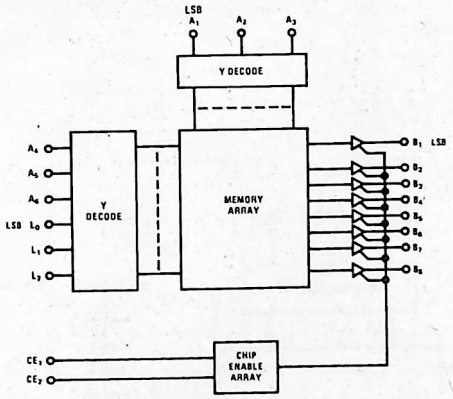
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

logic and connection diagrams



Dual-In-Line Package

Order Number MM4241J
or MM5241J
See Package 11
Order Number MM5241N
See Package 18

typical applications

TTL/MOS Interface

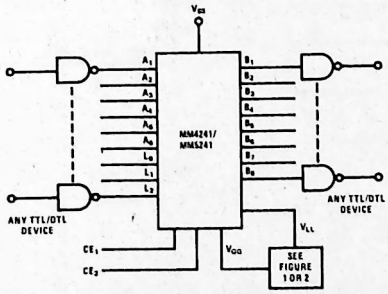


FIGURE 1. Power Saver for Small Memory Arrays

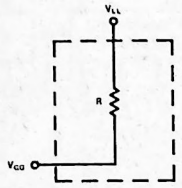
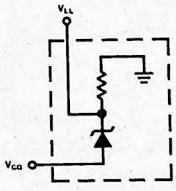


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME V_{LL} (MIN = −3V if
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If CE_1 = 1 and CE_2 = 1 outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = $V_S - 2V$; 0 = most negative voltage level = $V_{SS} - 4V$).

Note: For programming information see AN-100.

National Semiconductor

MOS ROMs

MM4242/MM5242 1024 x 8-bit ROM

general description

These static, 8192-bit ROMs are fabricated using N-Channel enhancement and depletion mode silicon gate technology. This provides complete DTL/TTL compatibility and single power supply operation.

Chip select inputs control the TRI-STATE® outputs and allow for memory expansion. The chip select code is programmed at the same time as the memory matrix and a code of 1:16 for the MM4242/MM5242 must be selected.

features

- Fully decoded
- Single +5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selection
- Maximum access time 450 ns
- Pin compatible with National's 4k and 16k ROMs

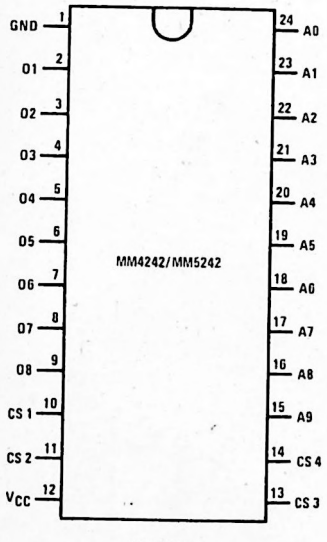
applications

- Microprogramming
- Control logic
- Random logic synthesis
- Table lookup

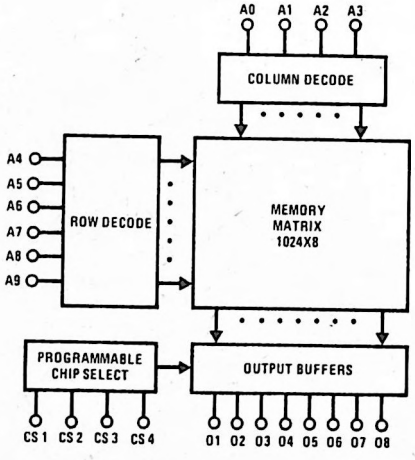
	Military	Commercial	Organization	Package
MM4242	X		1024 x 8	J
MM5242		X	1024 x 8	N, J

connection and block diagrams

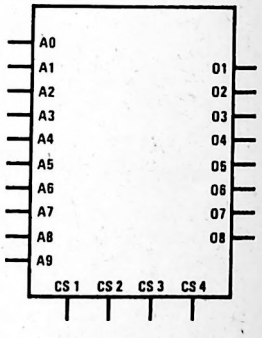
Dual-In-Line Package



TOP VIEW



logic symbol



National Semiconductor

MOS ROMs

PRELIMINARY

MM4246/MM5246 2048 x 8-bit ROM
MM4247/MM5247 4096 x 4-bit ROM

general description

These static, 16,384-bit ROMs are fabricated using N-channel enhancement and depletion-mode silicon-gate technology. This provides complete DTL/TTL compatibility and single power supply operation.

Chip select inputs control the TRI-STATE® outputs and allow for memory expansion. The chip select code is programmed at the same time as the memory matrix and a code of 1:8 for the MM4246/MM5246 and 1:4 for the MM4247/MM5247 must be selected.

features

- Fully decoded
- Single +5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selection
- Maximum access time 450 ns (MM5246, MM5247)
- Pin compatible with National 4k and 8k ROMs

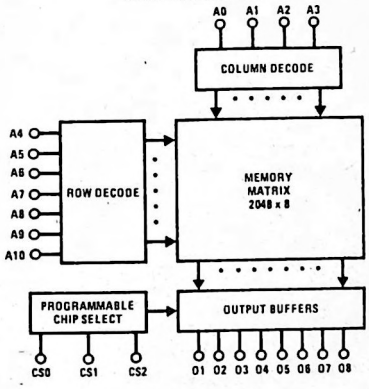
applications

- Microprogramming
- Control logic
- Random logic synthesis
- Table lookup

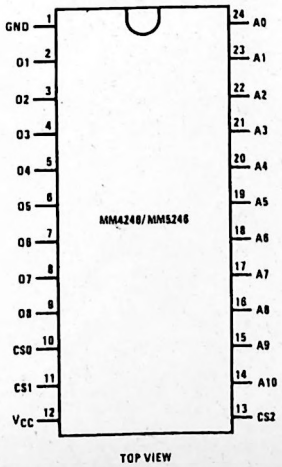
	Military	Commercial	Organization	Package
MM4246	X		2048 x 8	J
MM5246		X	2048 x 8	N, J
MM4247	X		4096 x 4	J
MM5247		X	4096 x 4	N, J

block and connection diagrams

MM4246/MM5246

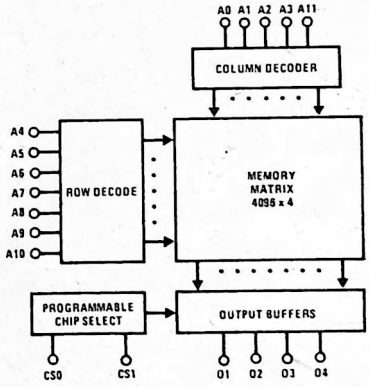

A0 A1 A2 A3
COLUMN DECODE
A4 A5 A6 A7 A8 A9 A10
ROW DECODE
MEMORY MATRIX 2048 x 8
PROGRAMMABLE CHIP SELECT
OUTPUT BUFFERS
CS0 CS1 CS2
O1 O2 O3 O4 O5 O6 O7 O8

Dual-In-Line Package

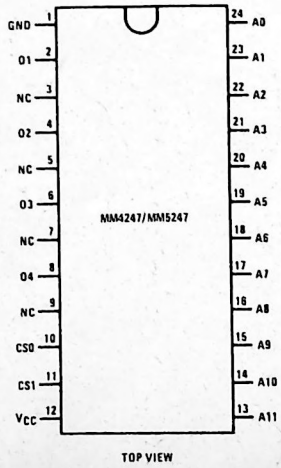


TOP VIEW

MM4247/MM5247



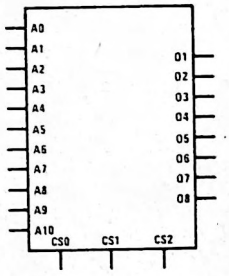
Dual-In-Line Package



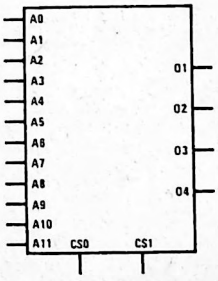
TOP VIEW

logic symbols

MM4246/MM5246



MM4247/MM5247



6

MOS ROMs

SK0003 sine/cosine look-up table kit

general description

The SK0003 Sine/Cosine Look-Up Table Kit consists of four MOS ROMs: three MM4210/MM5210's and one MM4220/MM5220-1024 bit static read only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing a low threshold technology.

THE SINE FUNCTION

The SK0003 implements the equation $\sin\theta = \sin M \cos L + \cos M \sin L$. Cos L was assumed to be 1 in the equation. However, it is a variable between 1 and 0.99998 and is a function of round off error. Worst case error is 1–5/8 bits in LSB at address 1415 (62.25°). The error increases from zero to .002% every 8 bits, therefore, the MM4220/MM5220 provides the error correction factor $\cos(M - 2.81°)\sin L$ in the equation $\sin\theta = \sin M + \cos(M - 2.81°)\sin L$. The circuitry to perform this function is shown in Figure 1. Additional information is available in *MOS Brief 10.*

THE COSINE FUNCTION

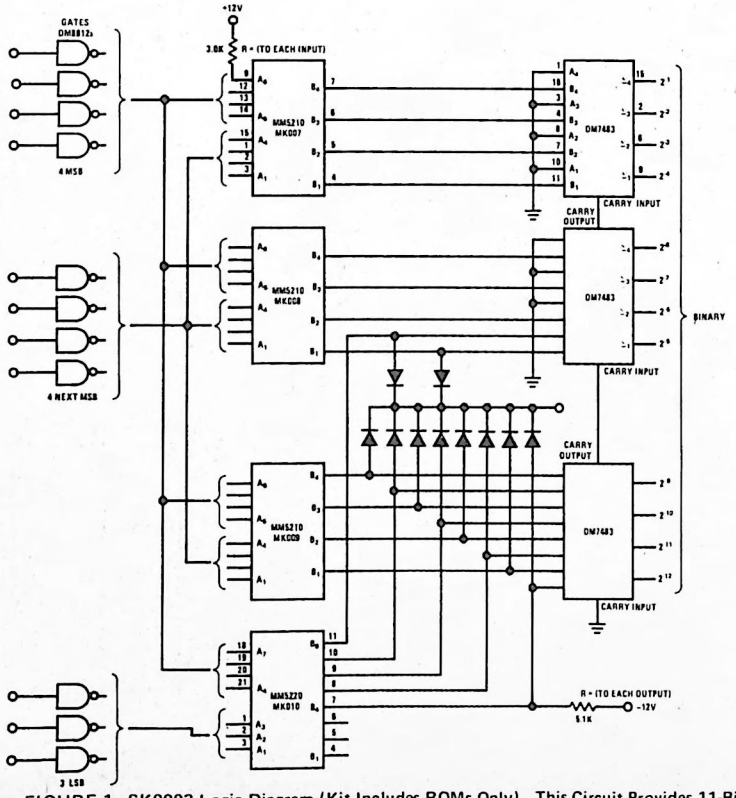
To generate the cosine function $\cos\theta = \sin(\theta - 90°)$, the input must be complemented and a logical "1" added. Figure 2A is a logic diagram of the circuitry used to provide the cosine function, as well as providing both sine and cosine functions in the same system. 11-bit resolution and 12-bit accuracy ±1–5/8-bits is achieved in this configuration.

A reduction in logic can be achieved as shown in Figure 2B if a loss in resolution of 1/2-bit in an 11-bit input or 1/4-bit in a 10-bit input is acceptable.

ELECTRICAL CHARACTERISTICS

Refer to the appropriate data sheet for each device shown in the figures. The devices noted are: MM4210/MM5210, MM4220/MM5220, DM5483/DM7483, DM7812/DM8812 and DM5486/DM7486.

logic diagram



Order Number SK0003C
or
Order Number SK0003M

FIGURE 1. SK0003 Logic Diagram (Kit Includes ROMs Only). This Circuit Provides 11-Bit Resolution and 12-Bit Accuracy in a θ to Sin θ Converter.

Bipolar ROMs

DM54187/DM74187(SN54187/SN74187)
1024-bit read only memory

general description

The DM54187/DM74187 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided; and when one is taken to the logical "1" state, it will cause all four outputs to go to the logical "1" state.

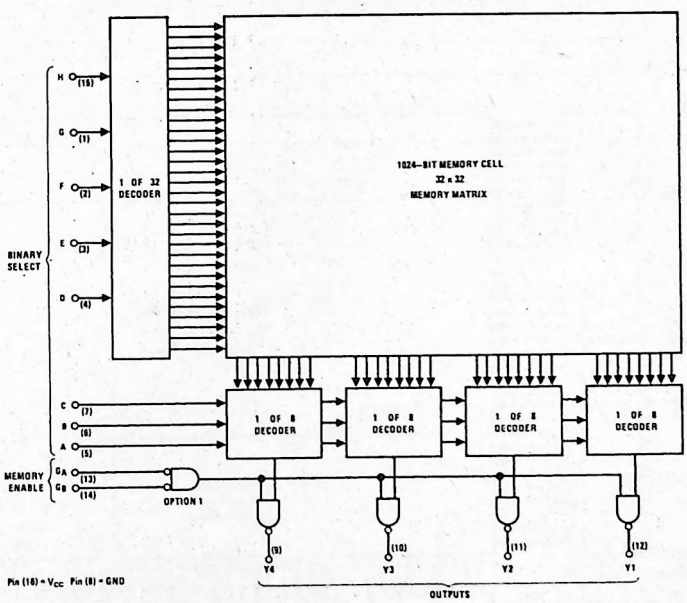
features

- 36 ns typical delay from address to output
- 20 ns typical delay from enable to output
- Open collector outputs for expansion

applications

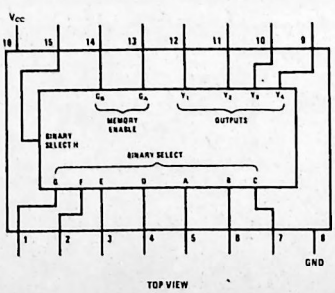
- Microprogramming
- Code conversions
- Look-up tables
- Use for any memory where content is fixed

logic diagram



connection diagram

Dual-In-Line Package



Order Number DM54187J
or DM74187J
See Package 10

Order Number DM74187N
See Package 15

Bipolar ROMs

DM54L187A/DM74L187A(SN54L187A/SN74L187A)
low power 1024-bit read only memory

general description

The DM54L187A/DM74L187A is a custom-programmed Read Only Memory organized as 256 4-bit words. Selection of the proper word is accomplished through the eight select inputs.

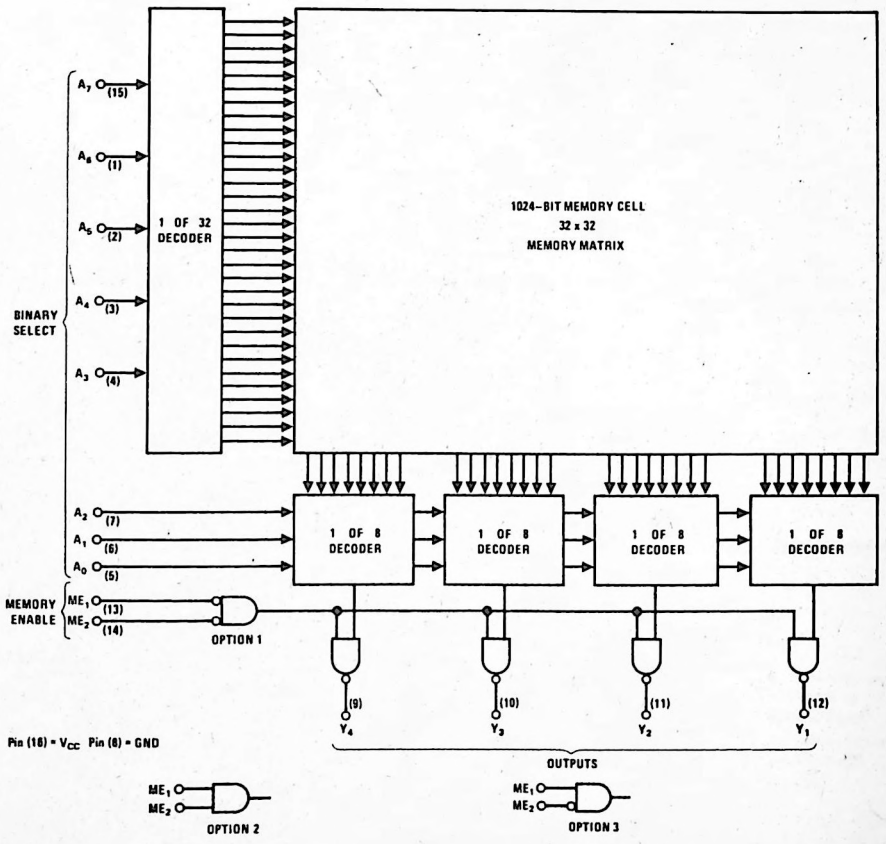
The "A" suffix is used to denote that full "tenth-power" technology has been employed in building this ROM.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the logical "1" state.

features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 90 mW
- Typical access time 85 ns
- Custom-programmed memory enable inputs
- Open-collector outputs

logic diagram



National Semiconductor

Bipolar ROMs

DM54S270/DM74S270 open-collector 2048-bit ROM
DM54S370/DM74S370 TRI-STATE® 2048-bit ROM

general description

These Schottky ROM memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

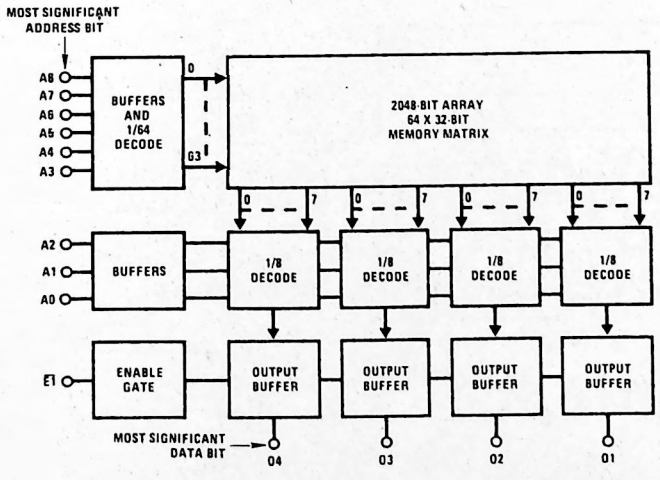
If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

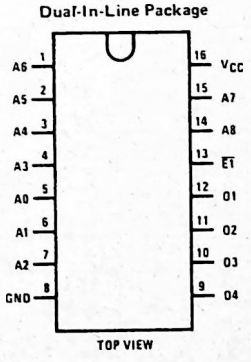
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S570 and DM74S571

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S270		X	X		N, J
DM74S370		X		X	N, J
DM54S270	X		X		J
DM54S370	X			X	J

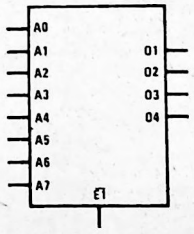
block diagram



connection diagram



logic symbol



7

National Semiconductor

Bipolar ROMs

PRELIMINARY

DM54S271/DM74S271 open-collector 2048-bit ROM
DM54S371/DM74S371 TRI-STATE® 2048-bit ROM

general description

These Schottky ROM's are organized in the popular 256 words by 8 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

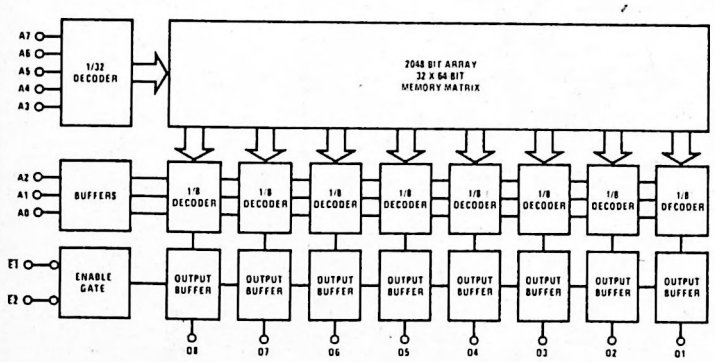
If either or both of the enable inputs is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  - Address access—60 ns max
  - Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- High density 20-pin package
- PROM mates are DM74S470 and DM74S471

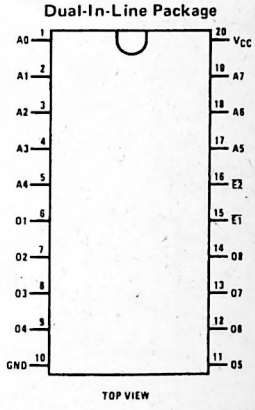
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S271		X	X		N, J
DM74S371		X		X	N, J
DM54S271	X		X		J
DM54S371	X			X	J

block diagram



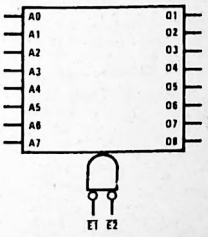
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



DM75S29/DM85S29 open-collector 8192-bit ROM
DM75S28/DM85S28 TRI-STATE® 8192-bit ROM

general description

These Schottky ROM memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

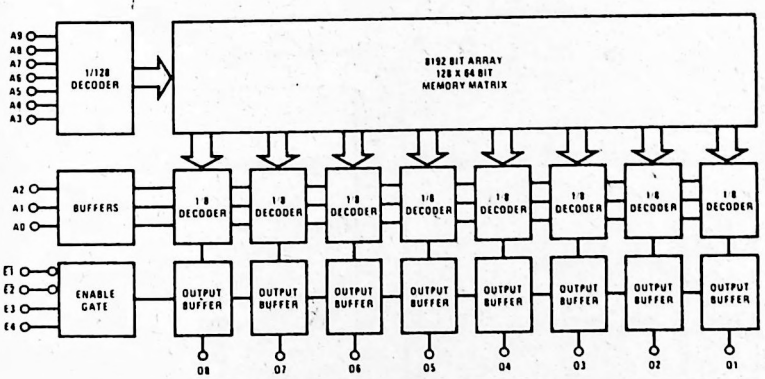
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  - Address access—70 ns max
  - Enable access—45 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM87S229 and DM87S228

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM85S29		X	X		N, J
DM85S28		X		X	N, J
DM75S29	X		X		J
DM75S28	X			X	J

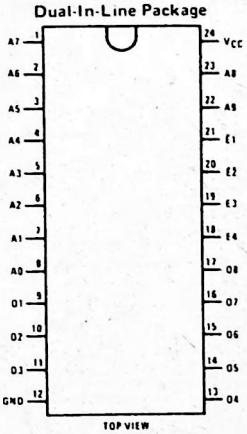
block diagram



The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

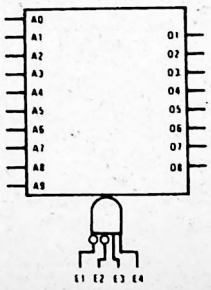
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



7

Bipolar ROMs

DM7575/DM8575, DM7576/DM8576 programmable logic array (PLA)

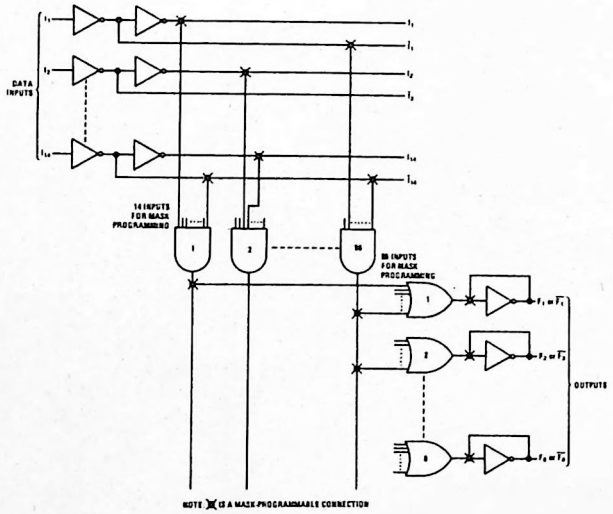
general description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

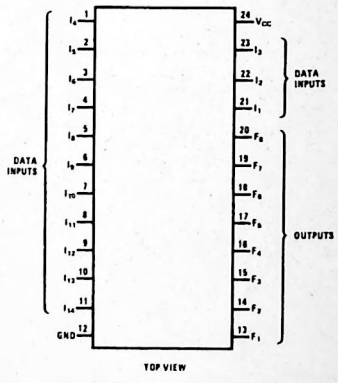
features

- A 2^{14}-by-8 (128k) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line Package



Order Number DM7575J, DM8575J, DM7576J or DM8576J
See Package 11
Order Number DM8575N or DM8576N
See Package 18

Bipolar ROMs

DM7596/DM8596 TRI-STATE®4096-bit bipolar ROM
DM7796 /DM8796 TRI-STATE 4096-bit bipolar ROM

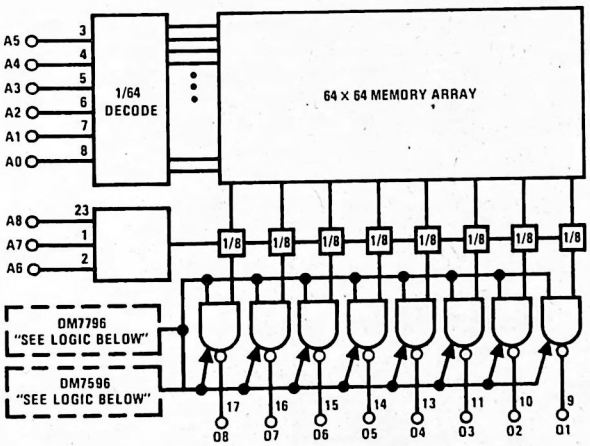
general description

The DM7596/DM8596 and DM7796/DM8796 are 4096-bit bipolar mask-programmable ROMs organized as 512 eight-bit words. Nine address inputs select the desired one-of-512 words. Four enable lines are used to either enable or disable the circuit. The two devices differ in the enable logic. Truth tables and logic diagrams for each device are shown below. TRI-STATE outputs allow for expansion to greater numbers of words without sacrifice in speed as would be evidenced by open-collector outputs.

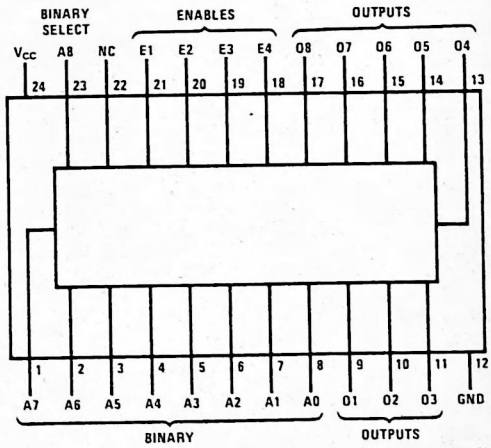
features

- Series 54/74 specification compatibility
- Pin compatible with Monolithic Memories MM5241/MM6241
- Typical address time 80 ns
- TRI-STATE outputs

logic and connection diagrams (Top View)



Dual-In-Line Package

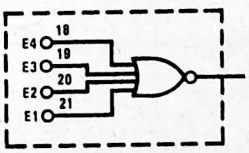

BINARY SELECT
ENABLES
OUTPUTS
VCC A8 NC E1 E2 E3 E4 O8 O7 O6 O5 O4
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
A7 A6 A5 A4 A3 A2 A1 A0 O1 O2 O3 GND
BINARY
OUTPUTS

Order Number DM7596J, DM8596J, DM7796J or DM8796J
See Package 11

Order Number DM8596N or DM8796N
See Package 18

logic diagrams and truth tables for enable circuitry

DM7596/DM8596

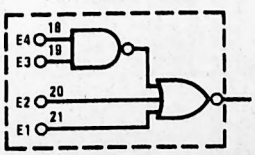


DM7596/DM8596

E1	E2	E3	E4	OUTPUT
0	0	0	0	Read Stored Data
1	X	X	X	Hi - Z
X	1	X	X	Hi - Z
X	X	1	X	Hi - Z
X	X	X	1	Hi - Z

X = Don't Care ENABLE = $\overline{E}_1 \cdot \overline{E}_2 \cdot \overline{E}_3 \cdot \overline{E}_4$

DM7796/DM8796



DM7796/DM8796

E1	E2	E3	E4	OUTPUT
0	0	1	1	Read Stored Data
1	X	X	X	Hi - Z
X	1	X	X	Hi - Z
X	X	0	X	Hi - Z
X	X	X	0	Hi - Z

X = Don't Care ENABLE = $\overline{E}_1 \cdot \overline{E}_2 \cdot E_3 \cdot E_4$

Bipolar ROMs

DM7597/DM8597 TRI-STATE® 1024-bit read only memory

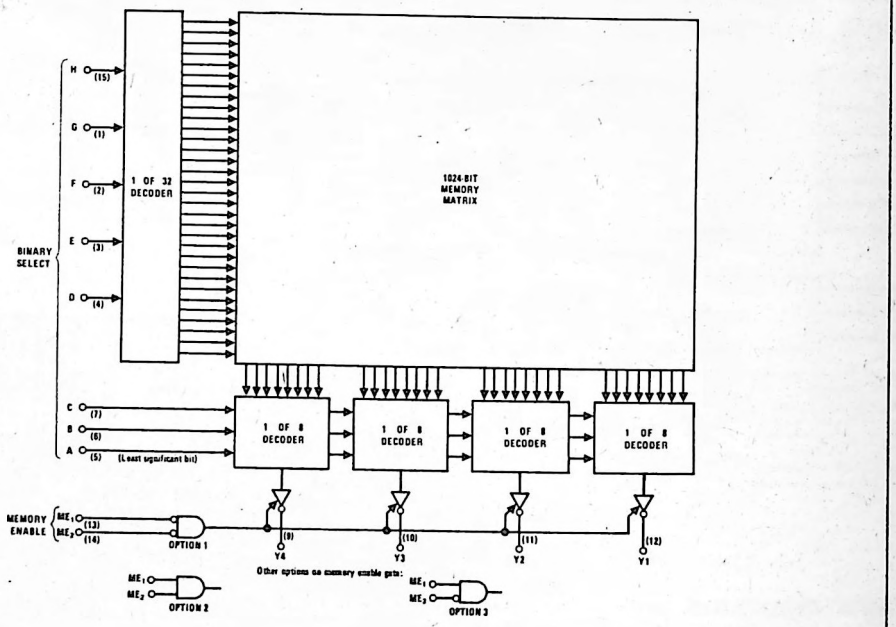
general description

The DM7597/DM8597 is a custom-programmed read-only memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs. Two overriding memory enable inputs are provided, which when mask-programmed in one of three options described will cause all four outputs to either read the normal memory contents or go to the "high impedance" state. In this state both the upper and lower output transistors are turned off. The outputs may therefore be paralleled to increase word capacity; since in the high-impedance state they present only a minimal load to the active output.

features

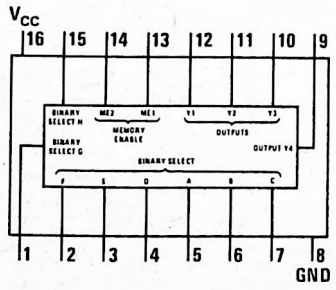
- Pin compatible with SN54187/SN74187
- 35 ns typical delay from address to output
- Can be expanded to 32,768 4-bit words by simple paralleling of outputs
- Programmable memory enable inputs

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM7597J or DM8597J
See Package 10

Order Number DM8597N
See Package 15

truth table

TABLE of Programmable Memory Enable Options

OPTION	ME1	ME2	OUTPUTS
1	0	0	Normal
	1	X	HIGH Impedance
	X	1	HIGH Impedance
2	1	1	Normal
	0	X	HIGH Impedance
	X	0	HIGH Impedance
3	1	0	Normal
	X	1	HIGH Impedance
	0	X	HIGH Impedance

X = don't care

National Semiconductor

Bipolar ROMs

PRELIMINARY

DM54S187/DM74S187 open-collector 1024-bit ROM
DM75S97/DM85S97 TRI-STATE® 1024-bit ROM

general description

These TTL compatible memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the logical "0" state, the outputs present the contents of the word selected by the address inputs.

If either or both of the enable inputs is raised to a logical "1" level, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROMs as well as ROMs.

features

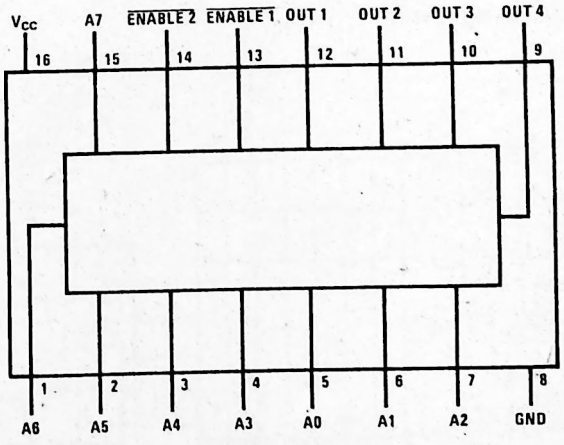
- Schottky clamped for high speed systems
- High speed

Enable to output delay—typical	15 ns
Address to output delay—typical	30 ns

- PNP inputs reduce input loading

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM54S187J or DM74S187J, DM75S97J or DM85S97J
See Package 10

Order Number DM74S187N or DM85S97N
See Package 15

7

DM7598/DM8598 TRI-STATE® 256-bit read only memory

general description

The DM7598/DM8598 is a customer programmed 256-bit read only memory, organized as 32 8-bit words. A 5-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the select inputs and blanks all outputs.

Although the DM7598/DM8598 can have its outputs tied together for word-expansion, the outputs are not open-collector, but rather the familiar totem-pole output with the capability of being placed in a "third-state." This unique TRI-STATE concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If, however, on all but one of the connected devices both the upper and lower output transistors are turned "OFF," then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7598/DM8598.

A typical system connection demonstrating expansion to greater numbers of words is shown in *Figure 1.* While it is true that in a TTL system open-collector gates could be used to perform the logic function of these three-state elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7598/DM8598 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

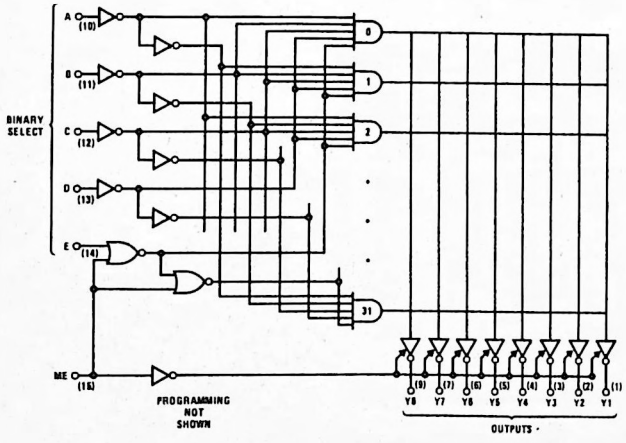
It is possible to connect as many as 128 DM8598s to a common bus line and still have adequate drive capability to allow fan-out from the bus. The example shown in *Figure 2* indicates how this guarantee can be made under worst-case conditions.

Figure 3 indicates how multiple packages can be used to increase word length.

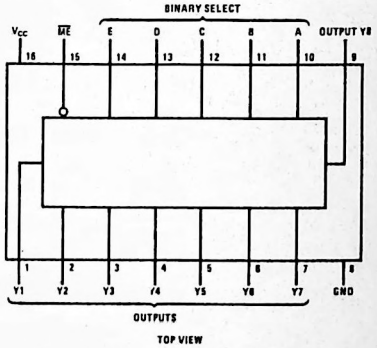
features

- Pin compatible with SN5488/SN7488
- Organized as 32 8-bit words
- Full internal decoding
- 26 ns typical access time
- 350 mW typical power dissipation
- Input clamp diodes
- Designed for bus-organized systems

logic and connection diagrams



Dual-In-Line Package



Order Number DM7598J or DM8598J
See Package 10

Order Number DM8598N
See Package 15

DM8678 bipolar character generator

general description

The DM8678 is a 64-character bipolar character generator with serial output, and packaged in a standard 16-pin DIP designed primarily for the CRT display marketplace. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing, and character line spacing which are normally done with extra packages.

Shifted characters can be generated by the on-chip subtractor.

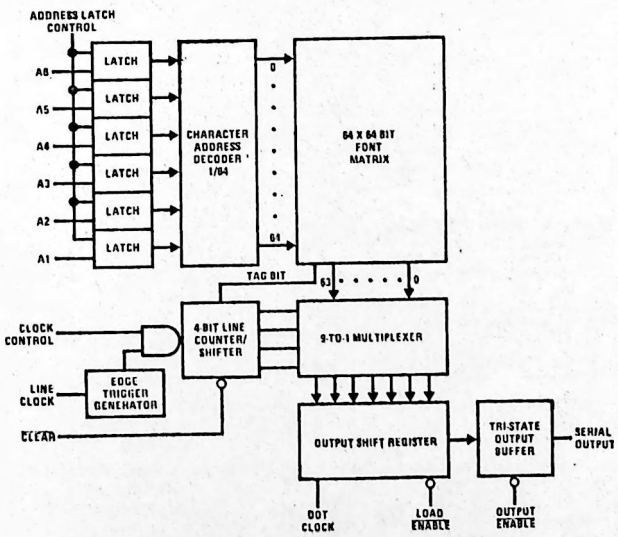
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "Fall Through" the latch. And when the address latch control signal goes low, the character addresses are latched

features

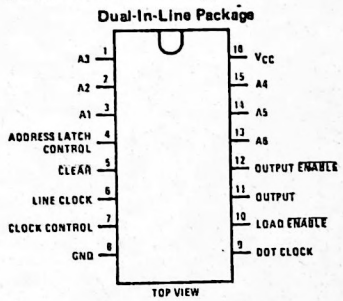
- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Shifted lower case descending characters
- Serial output
- 16-pin package
- 20 MHz clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE[®] output

	ROW SCAN	7 x 9	5 x 7	FONT	PACKAGE
DM8678BWF/	X	X		Upper Case Block Letters	N, J
DM8678CAE/	X	X		Shifted Lower Case Block	N, J
DM8678CAB/	X		X	Upper Case Block Letters	N, J
DM8678CAH/	X		X	Shifted Lower Case Block	N, J
DM8678CAD/	X	X		Kata Kana	N, J
DM8678BTK/	X	X		Upper Case Script Letters	N, J
DM8678CAS/	X	X		IBM 3741 Selectric	N, J

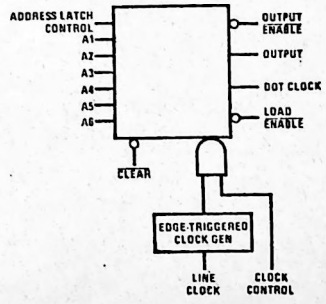
block diagram



connection diagram



logic symbol



7

DM76L97/DM86L97 TRI-STATE® low power 1024-bit read only memory

general description

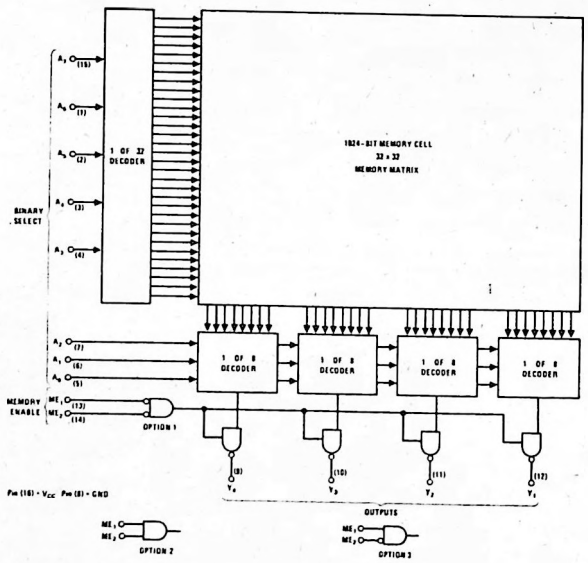
The DM76L97/DM86L97 is a custom-programmed Read Only Memory organized as 256 four-bit words. Selection of the proper word is accomplished through the eight select inputs.

Two overriding memory enable inputs are provided which when mask-programmed in one of the three options described will cause all four outputs to read either the normal memory contents or go to the high impedance state.

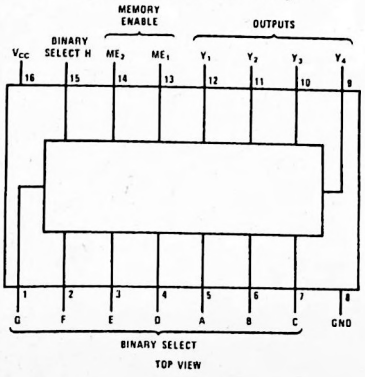
features

- Full tenth-power technology
- Pin compatible with SN54187/SN74187
- Typical power dissipation 75 mW
- Typical access time 70 ns
- Custom-programmed memory enable inputs
- TRI-STATE outputs

logic and connection diagrams



Dual-In-Line and Flat Package



Order Number DM76L97J or DM86L97J
See Package 10

Order Number DM76L97N or DM86L97N
See Package 15

Order Number DM76L97W or DM86L97W
See Package 28

Preliminary

DM77S201/DM87S201 open-collector 2048-bit ROM with latches
DM77S202/DM87S202 TRI-STATE® 2048-bit ROM with latches

general description

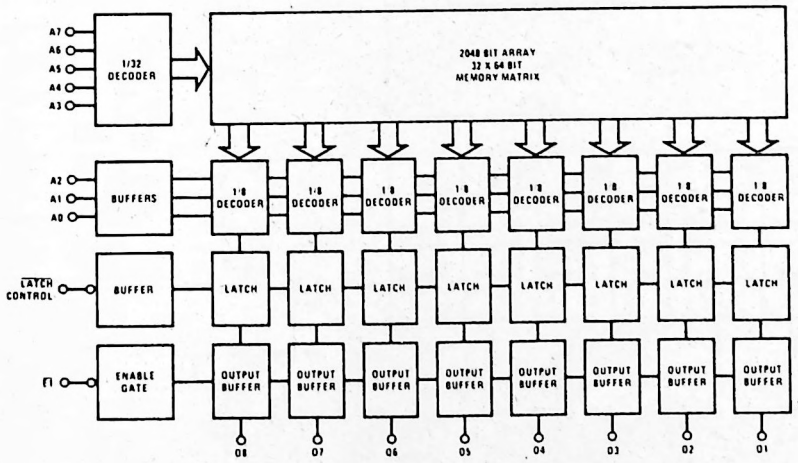
These Schottky ROM memories are organized in the popular 256 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word. An output latch control is provided. If the latch control pin is high, the data falls through to the output enable gate. If the latch control pin is low, the data is latched and the address may be changed without affecting the output data.

features

- Schottky-clamped for high speed
  - Address access—60 ns max
  - Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Open-collector or TRI-STATE® outputs
- High density 20-pin package
- PROM mates are DM87S221 and DM87S222

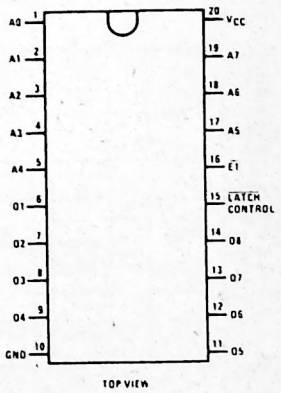
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S201		X	X		N, J
DM87S202		X		X	N, J
DM77S201	X		X		J
DM77S202	X			X	J

block diagram

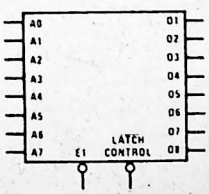


connection diagram

Dual-In-Line Package



logic symbol



7

DM77S95/DM87S95 open-collector 4096-bit ROM
DM77S96/DM87S96 TRI-STATE® 4096-bit ROM

general description

These Schottky ROM memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

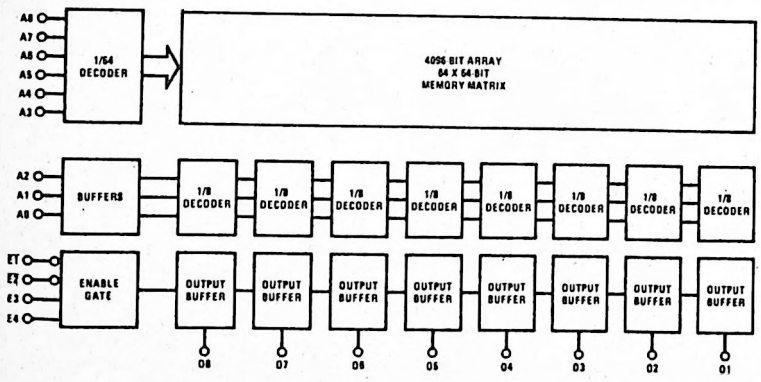
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  - Address access—65 ns max
  - Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM87S295 and DM87S296

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S95		X	X		N, J
DM87S96		X		X	N, J
DM77S95	X		X		J
DM77S96	X			X	J

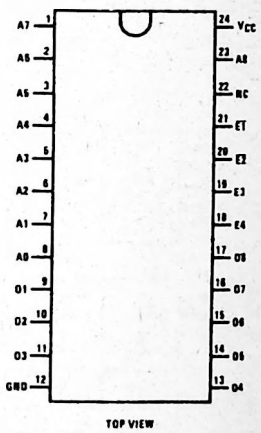
block diagram



The device is enabled when: $\overline{E}_1 \cdot \overline{E}_2 \cdot E_3 \cdot E_4$

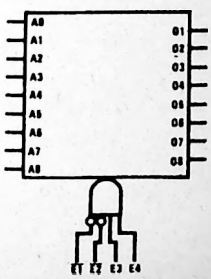
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Shift Registers

MM1402A, MM1403A, MM1404A, MM5024A
1024-bit dynamic shift registers

general description

The MM1402A,MM1403A,MM1404A,MM5024A 1024-bit dynamic shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. 5 MHz data rates are achieved by on-chip multiplexing. The clock rate is one-half the data rate; i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

All devices in the family can operate from +5V, –5V, or +5V, –9V power supplies.

features

- Guaranteed 5 MHz operation
- Low power dissipation .1 mW/bit at 1 MHz
- DTL/TTL compatible
- Low clock capacitance 125 pF
- Low clock leakage $\leq 1\ \mu A$
- Inputs protected against static charge
- Operation from +5V, –5V or +5V, –9V power supplies
- Seven standard configurations

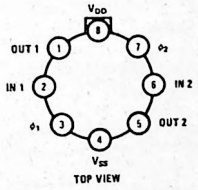
MM1402AD	Quad 256-bit
MM1402AN	Quad 256-bit
MM1403AH	Dual 512-bit
MM1403AN	Dual 512-bit
MM1404AH	Single 1024-bit
MM1404AN	Single 1024-bit
MM5024AH	Single 1024-bit with internal pull-down resistor

applications

- Radar and sonar processors
- CRT displays
- Terminals
- Desk top calculators
- Disk and drum replacement
- Computer peripherals
- Buffer memory
- Special purpose computers—signal processors, digital filtering and correlators, receivers, spectral compressors and digital differential analyzers
- Telephone equipment
- Medical equipment

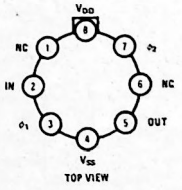
connection diagrams

Metal Can Package



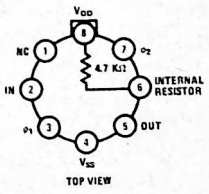
Order Number MM1403AH
See Package 23

Metal Can Package



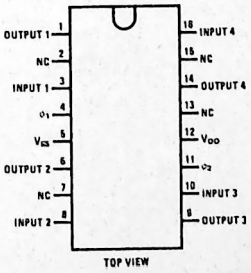
Order Number MM1404AH
See Package 23

Metal Can Package



Order Number MM5024AH
See Package 23

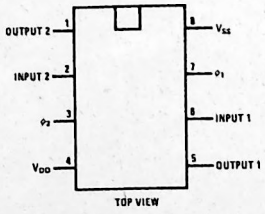
Dual-In-Line Package



Order Number MM1402AD
See Package 3

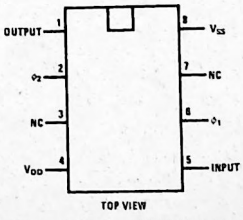
Order Number MM1402AN
See Package 15

Dual-In-Line Package



Order Number MM1403AN
See Package 12

Dual-In-Line Package



Order Number MM1404AN
See Package 12

8

Shift Registers

Revised January 1976

MM4025/MM5025 dual 1024-bit dynamic shift register
MM4026/MM5026 dual 1024-bit dynamic shift register
MM4027/MM5027 2048-bit dynamic shift register

general description

These 2048-bit dynamic shift registers are MOS monolithic integrated circuits using P-channel silicon gate technology. They employ a push-pull output for bipolar compatability and on-chip multiplexing to achieve a 6 MHz data rate. The clock rate is one-half the data rate, i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

The MM4025/MM5025 and MM4027/MM5027 have on-chip logic to load and recirculate data.

The MM4026/MM5026 has an individual logic-select line to load one of the two inputs on each of the 1024-bit registers.

features

- Bipolar compatibility — Standard +5V, −12V power supplies
- High frequency of operation — 6 MHz guaranteed
- Low power dissipation — 120 μW/bit at 1 MHz ϕ rate 0°C, guaranteed
- Low clock capacitance — 190 pF max
- Wide operating temperature range
  MM4025,MM4026,MM4027 −55°C to +125°C
  MM5025,MM5026,MM5027 0°C to 70°C

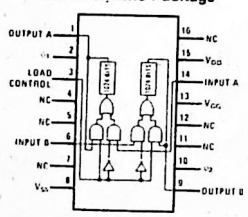
applications

- "Silicon store" replacement for drum and disc memories
- CRT displays
- Buffer memories

logic and connection diagrams

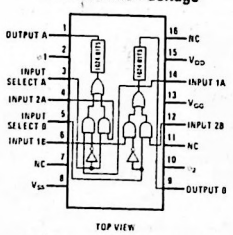
Military Temperature Range

Dual-In-Line Package



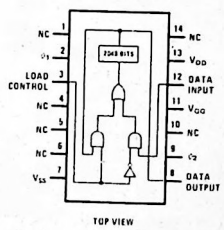
Order Number MM4025D
or MM5025D
See Package 3

Dual-In-Line Package



Order Number MM4026D
or MM5026D
See Package 3

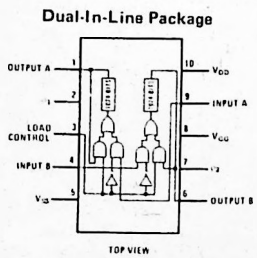
Flat Package



Order Number MM4027F
or MM5027F
See Package 26

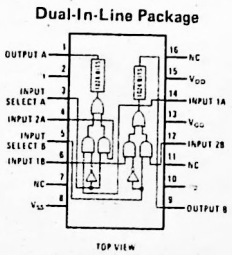
Commercial Temperature Range

Dual-In-Line Package



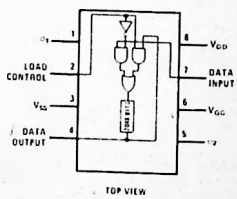
Order Number MM5025N
See Package 13

Dual-In-Line Package



Order Number MM5026N
See Package 15

Dual-In-Line Package



Order Number MM5027N
See Package 12

Shift Registers

MM5054 dual 64/72/80-bit static shift register

general description

The MM5054 dual 80-bit static shift register is a monolithic MOS integrated circuit utilizing silicon gate low threshold technology to achieve complete bipolar compatibility. The device has input and output taps that also provide register lengths of 64 or 72 bits.

The single phase bipolar compatible clock lines may be driven by any conventional DTL or TTL circuit. The registers may be operated as a dual register by connecting the clock lines A and B together, or as two independent registers. Two clock control lines provide independent logical control of the shift register clock lines.

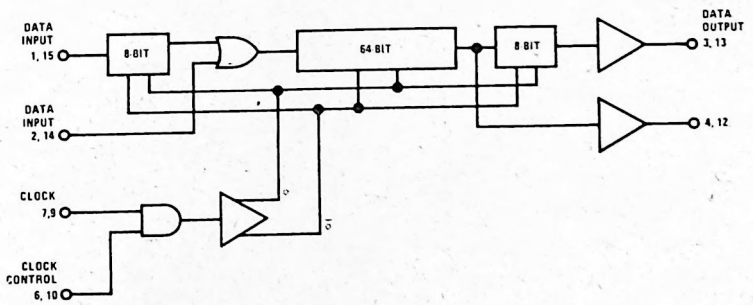
features

- Complete bipolar compatibility — DTL/TTL input/output and clock line compatibility without additional components
- Standard supplies — +5.0V, −12V
- High freq. operation — DC to 3.0 MHz typ
- Single phase clock — DTL/TTL compatible on-chip clock driver
- Low clock line capacitance — 8.0 pF max
- System flexibility — Split clock or common clock operation. Logical control of clock lines
- Low power dissipation — <600 μW/bit typ

applications

- Teletype data buffers
- Printer memory — 80, 128, 136, 144 bit lengths
- Telemetry and data sampling systems
- Serial memory storage

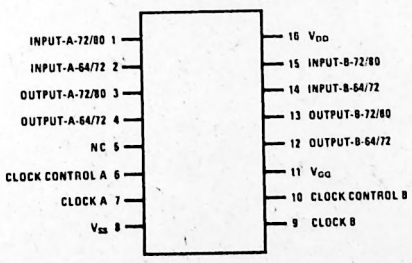
logic diagram



The unused data inputs and clock controls should be connected to V_{SS} to ensure proper operation.
Logic diagram shows 1/2 of the unit.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5054D
See Package 3
Order Number MM5054N
See Package 15

truth table

Positive Logic

CLOCK CONTROL	CLOCK
Low	Inhibited
High	Active

Shift Registers

MM4055/MM5055 quad 128-bit static shift register
MM4056/MM5056 dual 256-bit static shift register
MM4057/MM5057 512-bit static shift register

general description

The MM4055/MM5055, MM4056/MM5056, MM4057/MM5057 512-bit static shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. They have a guaranteed operating frequency of 1.0 and 1.5 MHz respectively, and an on chip clock generator allows TTL level clock driver for complete TTL compatibility.

features

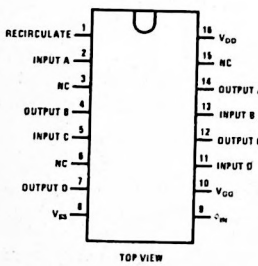
- Guaranteed operation
  - 1.5 MHz — 0°C to +70°C
  - 1.0 MHz — −55°C to +125°C
- Single TTL compatible clock, on chip clock generator
- Low clock capacitance — 10 pF (typ)
- Operates from +5.0V, GND, and −12V
- Three configurations
  - MM4055/MM5055 — Quad 128 bit
  - MM4056/MM5056 — Dual 256 bit
  - MM4057/MM5057 — Single 512 bit
- Internal recirculate

applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

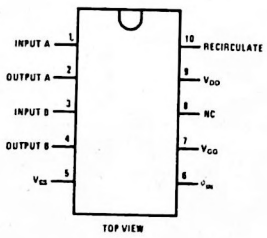
connection diagrams

Dual-In-Line Package



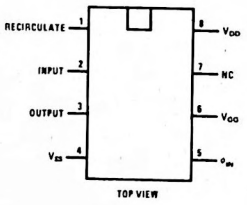
Order Number MM4055D or MM5055D
See Package 3
Order Number MM5055N
See Package 15

Dual-In-Line Package



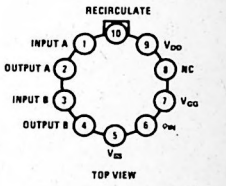
Order Number MM5056N
See Package 13

Dual-In-Line Package



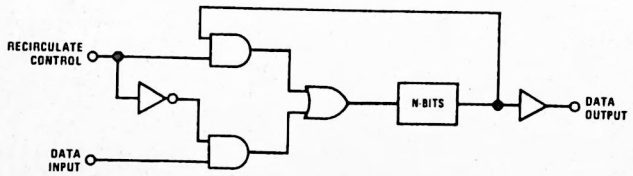
Order Number MM4057D or MM5057D
See Package 1
Order Number MM5057N
See Package 12

Metal Can Package



Order Number MM4056H or MM5056H
See Package 24

logic diagram



Shift Registers

MM5058 1024-bit static shift register

general description

The MM5058 is a monolithic 1024-bit static shift register utilizing a low threshold P-channel silicon gate technology to achieve bipolar compatibility. "Stream select" logic on the chip chooses between two inputs, facilitating external recirculate operation. This in addition to an internal clock-driver, thus providing a single external TTL/DTL clock, makes this device flexible and convenient to integrate into existing TTL/DTL or MOS systems.

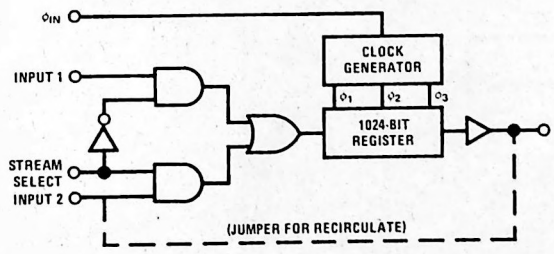
features

- Bipolar compatibility — All inputs, outputs, and clock interface directly with standard TTL/DTL circuits with no external components
- Single phase clock — On chip clock driver provides single TTL/DTL level clock with low input capacitance
- High frequency operation — DC to 1.5 MHz guaranteed
- Standard power supplies — +5.0V and −12V
- Small package — 8-pin mini DIP
- Low power consumption — 250μW/bit typ
- Stream select for easy external recirculate

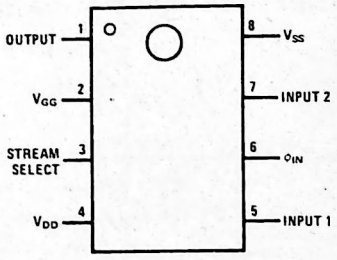
applications

- Sequential access memories
- Static buffer memories
- CRT refresh
- Delay lines
- Drum memory replacement

logic and connection diagrams



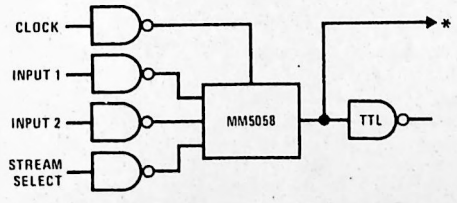
Dual-In-Line Package



TOP VIEW

Order Number MM5058D
See Package 1
Order Number MM5058N
See Package 12

ac test circuit



*PROPAGATION DELAYS MEASURED AT MM5058 OUTPUT.

truth table

STREAM SELECT	FUNCTION
LOGIC "0"	INPUT 1
LOGIC "1"	INPUT 2

Shift Registers

MM5060 dual 144-bit mask programmable static shift register

general description

The MM5060 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility. The device can be programmed by metal mask option to custom lengths from 125 to 144-bits in one bit increments.

Standard Lengths:

MM5060AA
Dual 128-Bit Shift Register/Accumulator
MM5060AB
Dual 132-Bit Shift Register/Accumulator
MM5060AC
Dual 133-Bit Shift Register/Accumulator
MM5060AD
Dual 144-Bit Shift Register/Accumulator

Custom Lengths:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as MM5060AD/D which is a 0°C to +70°C dual 144-bit shift register/accumulator in an 8-lead cavity dual-in-line package. Pattern codes are assigned by National upon entry of order.

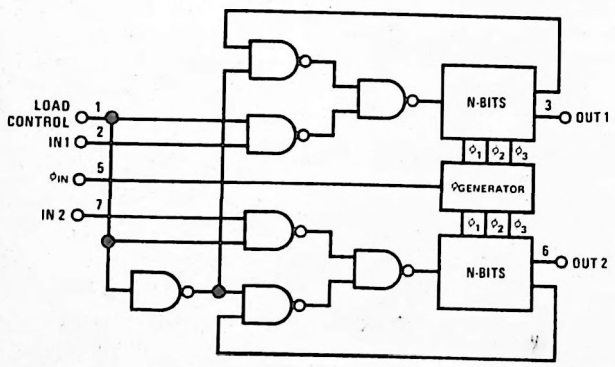
features

- Complete bipolar compatibility — input/output and clock input completely DTL/TTL compatible without additional components
- Standard Supplies +5V, −12V
- High frequency operation — DC to 3.0 MHz typical
- Single phase clock — DTL/TTL compatible on chip clock
- Low clock line capacitance 6.0 pF max.

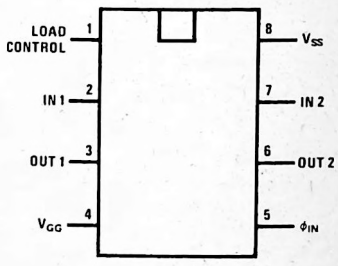
applications

- Printer memory — any length from 125 to 144-bits per line
- Telemetry systems and data sampling
- Serial memory storage

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5060AA/D, MM5060AB/D, MM5060AC/D, MM5060AD/D or MM5060XX/D
See Package 1

Order Number MM5060AA/N, MM5060AB/N, MM5060AC/N, MM5060AD/N or MM5060XX/N
See Package 12

truth table

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

Shift Registers

MM5061 quad 100-bit static shift register

general description

The MM5061 quad 100-bit static shift register is a MOS monolithic integrated circuit using silicon gate technology to achieve bipolar compatibility. It has a guaranteed operating frequency of 1.5 MHz and an on-chip clock generator.

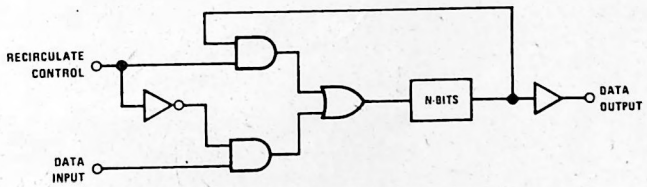
features

- Guaranteed 1.5 MHz operation
- Single TTL compatible clock on chip clock generator
- Low clock capacitance 10 typ, 14 max.
- Operates from +5V, GND, and -12V
- Configuration Quad 100-bit
- Internal recirculate

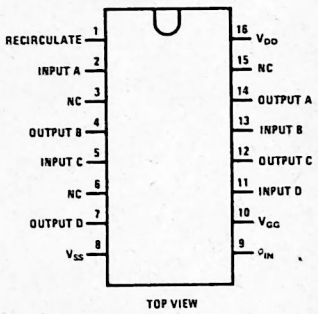
applications

- CRT displays
- Terminals
- Disk and drum replacements
- Buffer memory

logic and connection diagrams

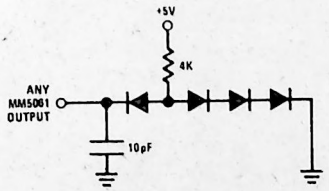


Dual-In-Line Package



Order Number MM5061D
See Package 3
Order Number MM5061N
See Package 15

test circuit



truth table

RECIRCULATE CONTROL	FUNCTION
1	Data Recirculates
0	Register Accepts Input Data

National Semiconductor

Memory Systems

Memory and Computer Groups:

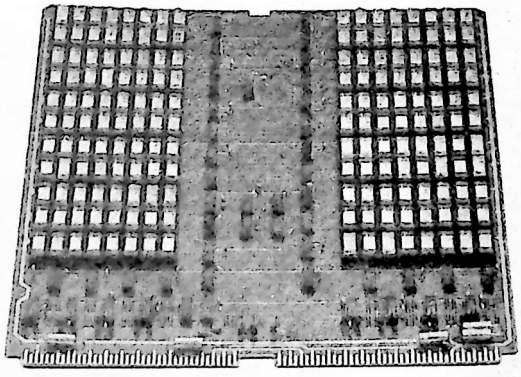
OEM Memory Systems
370-Add-On Memory Systems
Memory Components
MicroComputer Systems
Large Computer Systems

Memory Technology

National's memory systems take full advantage of the growing technology in semiconductor random access memories. With the 18- and 22-pin 4k RAM now in volume production, this technology already provides higher performance at lower cost than "core" memory. And it promises even greater advantages as National continues to make improvements in speed, compactness, and cost.

World's Largest Memory Supplier

At the forefront of semiconductor memory technology and now the world's largest supplier, National produces the most cost-effective memory components and systems available. Since memory specialists at National are aware of OEM and end-user needs within a growing technology, National's OEM memories give you maximum performance with minimum obsolescence. The memories you purchase from National today will be available tomorrow *with improved cost-performance ratios* reflecting new advances in component technology.



370 "Add-on" Memories

Fully committed to the memory system market, National has developed a standard line of IBM-compatible "add-on" semiconductor memories. These memories range in size from 256k bytes for the 370-135 to 8M bytes for the 370-168. Available at lower cost than comparable memories, these systems include "large computer" features such as error checking and correction, CPU "hand-shaking," independent cooling, plug-in compatibility and ultra-high reliability.

Memory Specialists

National's memory systems group is staffed by a team of specialists in OEM and end-user memory design and production. Cooperating closely with semiconductor component technologists and computer system specialists, our memory systems group has both the expertise and the technology to provide you with reliable memories utilizing state-of-the-art components at the lowest possible cost.

Standard Memories

National's standard product line offers you a selection of reliable memories for a wide range of OEM and end-user applications. Including both "add-on" and "add-in" versions for specific minicomputers and micro-processors, the standard product line features memories designed for core memory card replacement, alpha-numeric displays and general use in communications, instrumentation, intelligent terminals, and many other applications. These memory products are described on the following pages.

Custom Memories

If the memory you need isn't presently available in our standard line, our memory systems team will design one to meet your specifications. After your first prototypes are built and fully tested, you can either have National build your memory systems or build them in your own plant with a licensing agreement: National will provide the first systems and the design, and you may use National as an alternate source.

Reliability

National has an outstanding reputation for reliability, and our memory systems are no exception. *Every* National memory is thoroughly inspected, "burned in" and tested at both the component and system levels before shipment.

State-of-the-Art Design

As improved memory technology becomes available, National memories are automatically design-updated. Custom memories are design-updated, with customer approval, with no interruption in production. This assures you of a memory system that is constantly competitive in cost and performance, without additional capital investment or design cost.

NS3-1 Bulk Storage Memory

A compact, 256k byte random access memory system with integral power supply and cooling in a standard 5.25″ x 19″ rack-mountable enclosure. The NS3-1 combines fully engineered reliability with designed-in flexibility. It is highly cost effective in a wide range of applications, including graphics terminals, PBX, mini- and microcomputers, time-share systems, process control, automatic testers, and medical analyzers.

Features

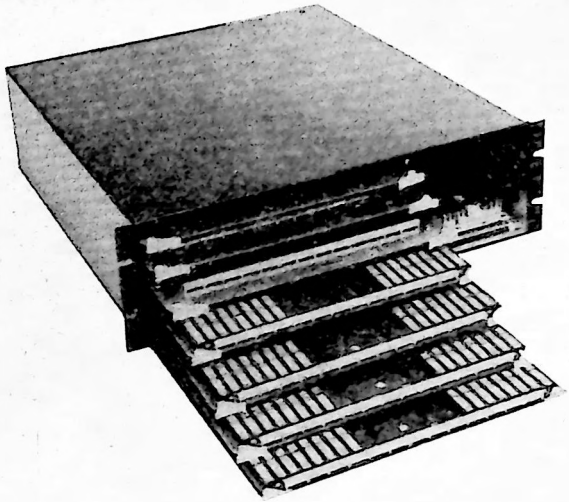
High Speed	280 ns access, 430 ns read or write cycle
Core-Compatible Timing	650 ns cycle
Error Check and Correction	Two or four bytes, optional
Parity	Checking and/or generation
Byte Control	One, two, or four byte control
Modular Memory	64k byte modules, 256k bytes max.
Custom Interface	For individual processors
Refresh Control	Synchronous or asynchronous
Data Bus	Unidirectional or bidirectional

Modular Design

The NS3-1 is part of National's growing NS3 family of modular bulk storage systems. These systems are slated for continuous technological update and development of additional compatible modules to provide enhanced performance, capacity and economy.

Specifications

Capacity	256k x 11 bit bytes maximum 1, 2, or 4 byte words
Operating Modes	Read, Write, Read/Modify/Write; Partial-Store with ECC option
Cycle Times:	
standard	280 ns access, 430 ns cycle, 650 ns split cycle
core-compatible	280 ns access, 650 ns cycle, 750 ns split cycle
ECC option	425 ns access, 650 ns cycle, 795 ns split cycle
Interface	TTL-compatible
Power	Integral power supply, 115/208 VAC, 50/60 Hz
Dimensions	Standard 19″W x 22.5″L x 5.25″H
Temperature	0–50°C, operating



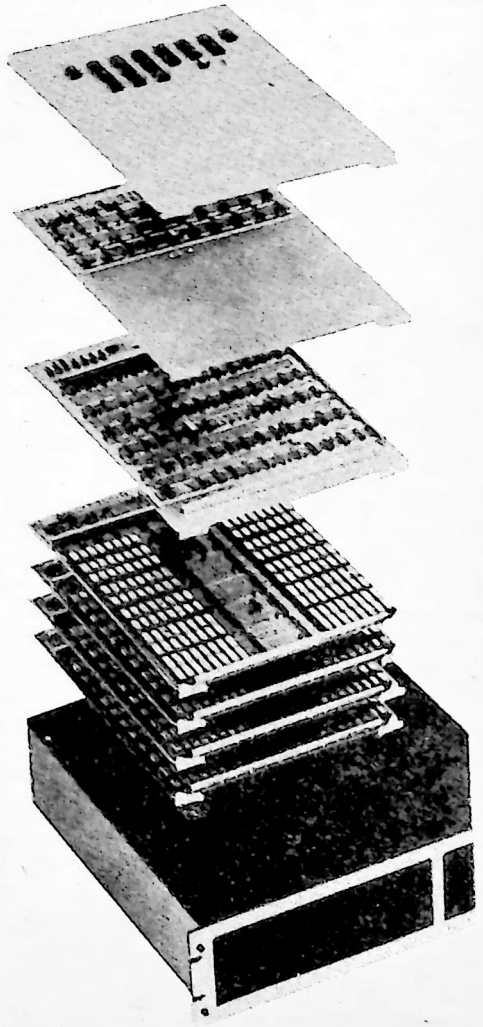
Custom Interface Card– For specially designed interface; breadboard available for customer design

Special Features Card– Offers special options, including ECC, 4-byte word structure, and others

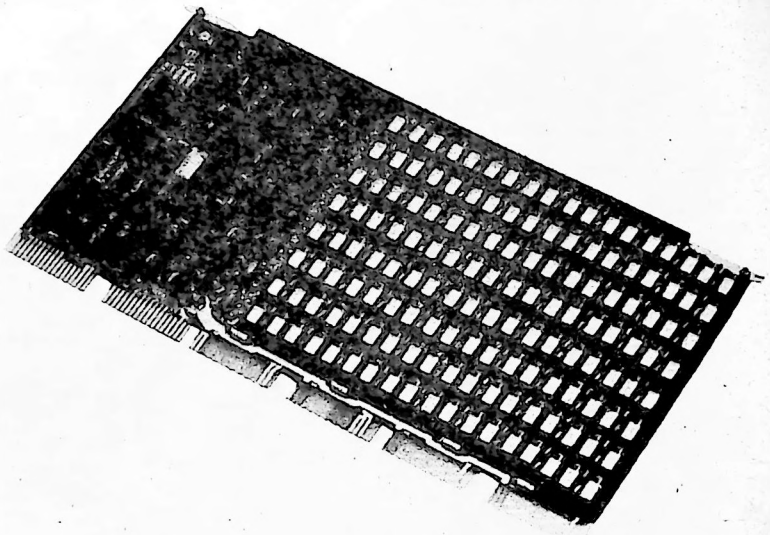
Timing and Control Card– Includes master control, parity and refresh circuits control logic

Memory Storage Cards– Up to four Memory cards, each with 64k bytes, various word structures optional

Enclosure & Power Unit– Standard 5.25" x 19" rack-mountable chassis with integral power supply and cooling. Table-top cabinet and interface cables optional



NS11 **Memory Series** 32K x18 Bits



A family of double-density random access memory cards that are fully hardware and software compatible with Digital Equipment Corporation's line of PDP11 processors. Direct plug-in replacement memory for models -/04, -/05, -/10, -/34, -/35, -/40, -/45, -/50, and -/55 is available.

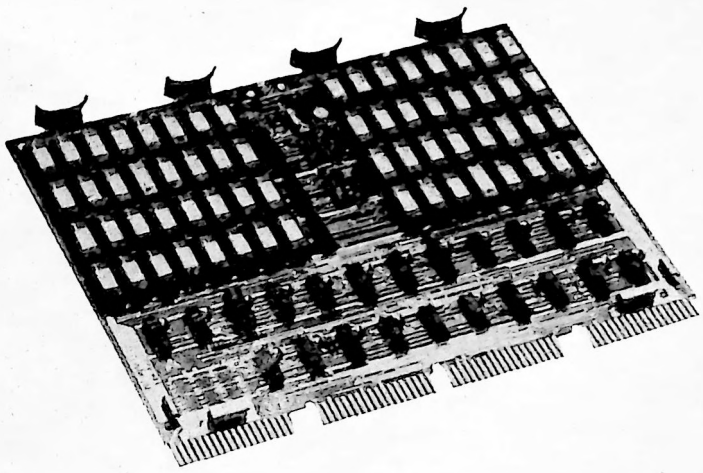
Features

High Speed	375 ns access, 525 ns full cycle
Double-Density	32k words on a single card
Compatibility	Plug-in replacement; can be intermixed with DEC memory cards
Expandable	To 128k words
Parity Bits	On card

Specifications

Capacity	32k x 18 bits, expandable to 128k
Address	Jumper-select in 32k blocks
Operating Modes	Read, Write
Cycle Times:	
access	375 ns for Read, Write or Refresh
full cycle	525 ns for Read or Write
Interface	Hardware and software compatible with PDP11 series (except PDP11/03) processors
Power	Compatible with host system, all voltages ±5%
Dimensions	15.69″W x 8.88″L
Temperature	0–50°C, operating

NS11/03 **Memory Card** 16K x 16 Bits



A double-density random access memory card that is fully hardware and software compatible with LSI11 and PDP11/03 processors. The NS11/03 is a direct plug-in replacement for four 4k cards.

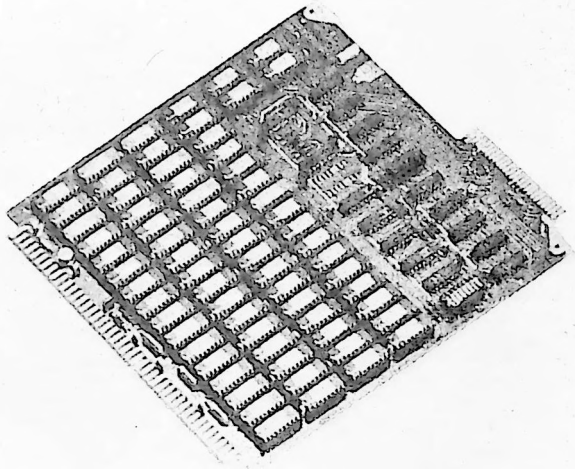
Features

High Speed	400 ns access, 1100 ns full cycle
Double-Density	16k card replaces four 4k cards
Compatibility	Plug-in replacement; can be intermixed with DEC memory cards
Expandable	To 24k or 32k
Low Power	11.5 W/card
High Reliability	

Specifications

Capacity:	
basic card	16k x 16 bits
option	8k x 16 bits, by depopulation
Address	Jumper-selectable in 4k blocks
Operating Modes	Read, Write, Read/Modify/Write, Refresh
Cycle Times:	
access	400 ns
cycle	1100 ns for Read-Modify-Write, 800 ns for Read, Write or Refresh
Interface	Hardware and software compatible with PDP11/03 series processors
Power	+5V at 1.1A; +12V at 0.5A
Dimensions	10.44″W x 8.9″L
Temperature	0–70°C.

NS21 **Memory Card** 16K x 17 Bits



A double-density random access memory card for replacing two 8k cards in the Hewlett-Packard 21MX family of computers. Also for general use, the NS21 features easy flexibility for large or small systems. Use with HP21MX or NS21 Control Card.

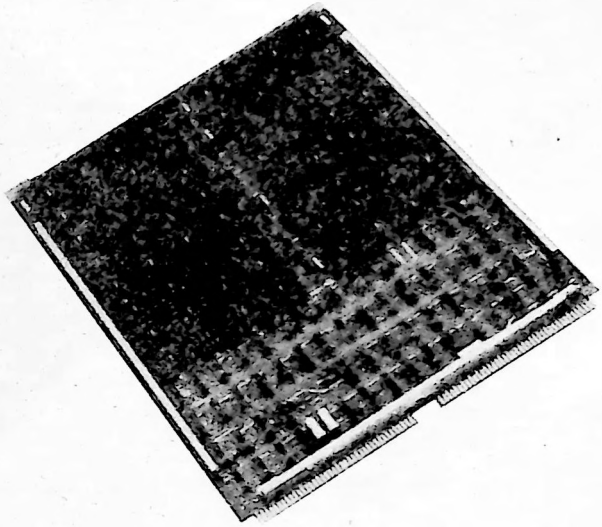
Features

High Speed	335 ns access, 650 ns cycle
Double-Density	16k card replaces two 8k cards
Compatibility	Plug-in replacement; can be intermixed with HP memory/control cards
Expandable	to 192k words
DIP-Switch Address Select	
Extended Warranty	1 year

Specifications

Capacity:	
basic card	16k x 17 bits, expandable to 192k
option	8k x 17 bits, expandable to 128k
Address	DIP-switch-selectable in 4k blocks
Operating Modes	Read, Write, Refresh
Access and Cycle Times:	
access	335 ns from address 290 ns from clock
full cycle	650 ns
Interface	Standard TTL, hardware and software compatible with HP21MX series processors
Power	±5V, ±12.4V; all voltages ±5%
Dimensions	7.75″W x 8.92″L
Temperature	0–70°C, operating

NS32 **Memory Card** 32K x 16 Bits



A random access memory card designed for video-graphics, computer language storage and other cyclic applications. Special features include programmable address formats, byte select, on-board refresh, and a high speed write-mask mode for video-compatible read/update cycles.

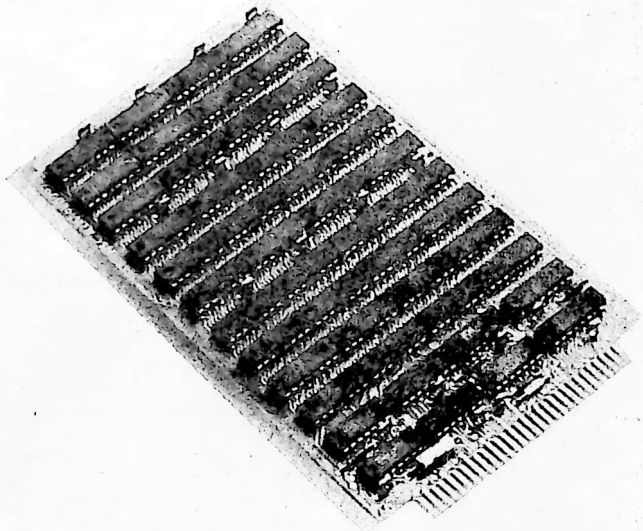
Features

High Speed	380 ns Read or Write cycle
Write-Mask Mode	Writes only "zeros" or "ones"
Programmable Format	Selects 32k x 16 or 16k x 32 bit
On-Board Refresh	Synchronous
Simple Interface	Self-contained, TTL-compatible, standard NS3 card size
Low Power	35 W/card

Specifications

Capacity	32k x 16, 16k x 32 (16 bits write) programmable
Operating Modes	Read, Write or Masked Write (copies only "zeros" or only "ones" into memory)
Access and Cycle Times:	
read or write	340 ns access, 380 ns cycle
Interface	TTL-compatible
Power	+12V, +5V, −5V (optional +15V, +5V, −5V)
Dimensions	11.8"W x 15.4"L
Temperature	0–50°C, operating

NS400-N series — Memory Cards 4K x 8, 9 or 10 Bits



A selection of high performance, random access memory cards that use static NMOS RAM's to eliminate clocks and refresh. Designed for simple interfacing and modular flexibility, each 400-N card is a compact, self-contained 4k memory system.

Features

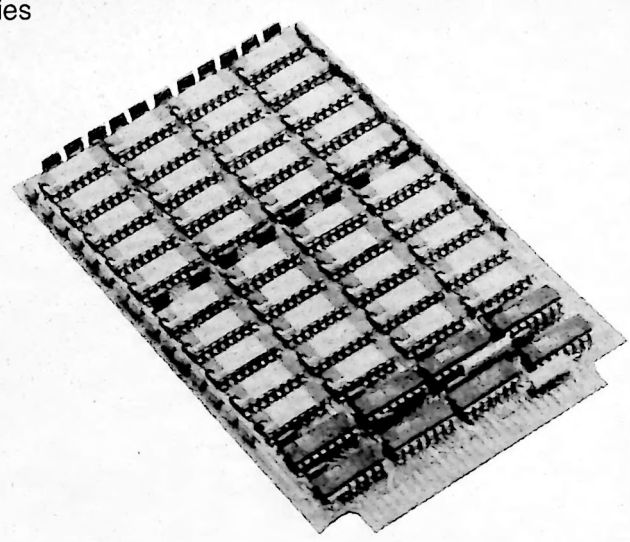
High Speed	300 or 550 ns access time
Static RAM's	No clocks or refresh circuits
Simple Interface	Single +5V supply; TTL compatible I/O
Expandable	4k x 8, 9 or 10 bits, expandable to 32k
Compact	3.93″ x 6.3″ cards
Low Power	5 W/card

Specifications

Capacity:	
basic card	4k x 8, 9 or 10 bits, optional
system	Expandable to 32k in 4k increments
Address	Jumper-selectable in 4k blocks
Operating Modes	Read or Write
Cycle Times:	
NS400-NS	550 ns, Read or Write
NS400-NH	300 ns, Read or Write
Interface	Standard TTL-compatible
Power	+5V at 1A, each card
Dimensions	3.93″W x 6.3″L
Temperature	0–50°C, operating

NS400-C series

Memory Cards 4K x 8, 9 or 10 Bits



A selection of compact, self-contained 4k memory cards that use static CMOS RAM's to eliminate refresh and minimize power usage in battery back-up applications. Choice of high speed, low power NS 400-CL version or ultra-low power NS 400-CC version. Simple interfacing, modular flexibility.

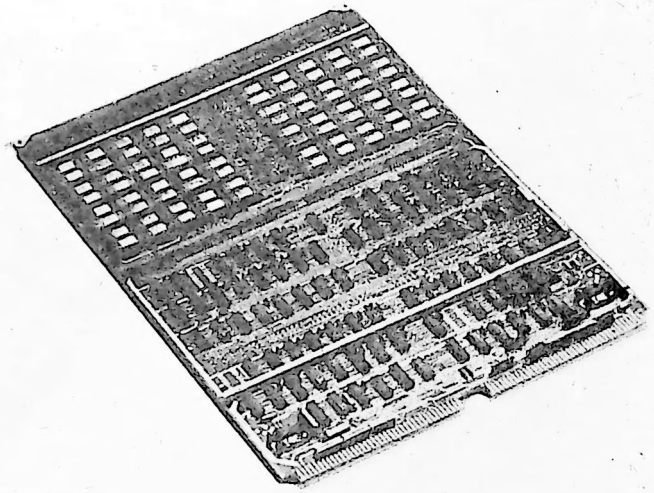
Features

High Speed Static RAM's	400 or 575 ns access time No clocks or refresh circuits
Simple Interface	Single +5V supply
Expandable	4k x 8, 9 or 10 bits, expandable to 32k
Compact	3.93″ x 6.3″ cards
Ultra-Low Power	Less than 450 mW operating, 5 mW standby (-CC)
Wide Voltage Range	3.5 to 5.5V (400-CC)

Specifications

Capacity:	
basic card	4k x 8, 9 or 10 bits, optional
system	Expandable to 32k in 4k increments
Address	Jumper-selectable in 4k blocks
Operating Modes	Read or Write
Cycle Times:	
NS400-CL	400 ns access, 500 ns cycle
NS400-CC	575 ns access, 700 ns cycle
Power	
NS400-CL	+5V; 1.5W, max.
NS400-CC	+3.5V to 5.5V; 0.5W, max.
Dimensions	3.93″W x 6.3″L
Temperature	0–70°C, operating

NS3000-1 **Memory Card** 16K x 20 Bits



A versatile random-access memory card, plug-in compatible with MM3000 core memory cards. Switch-selectable options for performance and easy interface. Applications: mainframes, mini and microcomputers, terminals, data entry, etc.

Features

High Speed	280 ns access, 450 ns cycle
Flexibility	1 or 2 byte words, byte control
Expandable	To 8-card system
Refresh	On-board control circuits; three modes
Special Options	Late data, parity generation, parity check, bi-directional bus
Low Power	35W maximum dissipation

Specifications

Capacity:	
each card	16k x 16, 18 or 20 bits or 32k x 8, 9 or 10 bits
8-card system	128k x 20 or 256k x 10 bits, max.
Address	3-bit extension, on-board drivers
Operating Modes	Read, Write, Read/Modify/Write, Refresh
Access and Cycle Times:	
access	280 ns
cycle, standard	450 ns full cycle, 650 ns split cycle
cycle, core compatible	650 ns full cycle, 750 ns split cycle
refresh	Synchronous, asynchronous or address-keyed
Interface	TTL-compatible; plug-in compatibility with MM3000 series
Power	Standard +12V, +5V, −5V Optional +15V, +5V, −15V
Dimensions	11.75″W x 15.40″L
Temperature	0–50°C, operating

The "Make or Buy" Decision

If you can't decide whether to build your own memory or have National build it for you, consider the following reasons why our customers have chosen National Semiconductor Memory Systems:

Design Expertise
We *specialize* in memory systems. Utilizing National's memory expertise leaves your engineers free to do what they do best.

Technology Advances
We provide continual design update to guarantee against obsolescence.

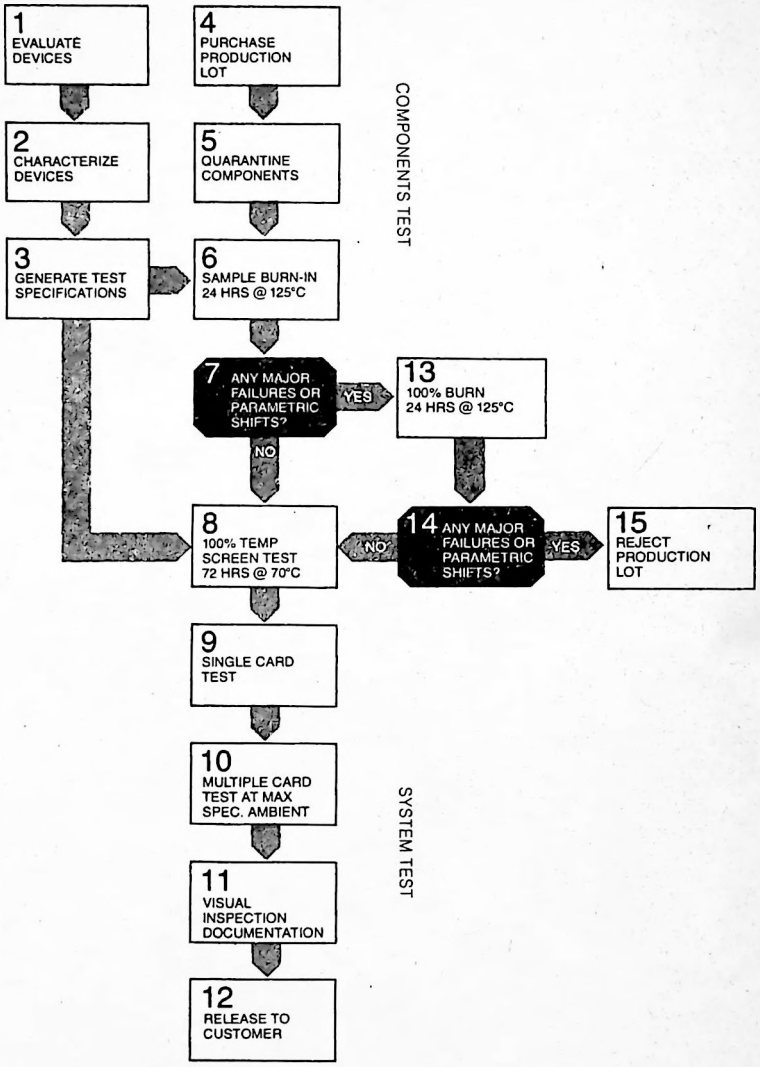
Component Availability
Our long-lead procurement cycle and second-sourcing of all components assures uninterrupted memory production.

Inventory
We minimize your inventory and simplify your purchasing by establishing production rates that match your needs.

Quality
Our extensive inspection, burn-in and testing procedures have required substantial investment, but they are essential to guarantee the reliability of National memories.

Cost-Performance
Our memories provide the highest performance at the lowest cost.

National's Memory Systems Testing


1 EVALUATE DEVICES
2 CHARACTERIZE DEVICES
3 GENERATE TEST SPECIFICATIONS
4 PURCHASE PRODUCTION LOT
5 QUARANTINE COMPONENTS
6 SAMPLE BURN-IN 24 HRS @ 125°C
COMPONENTS TEST
7 ANY MAJOR FAILURES OR PARAMETRIC SHIFTS?
YES
NO
13 100% BURN 24 HRS @ 125°C
8 100% TEMP SCREEN TEST 72 HRS @ 70°C
14 ANY MAJOR FAILURES OR PARAMETRIC SHIFTS?
NO
YES
15 REJECT PRODUCTION LOT
9 SINGLE CARD TEST
10 MULTIPLE CARD TEST AT MAX SPEC. AMBIENT
11 VISUAL INSPECTION DOCUMENTATION
12 RELEASE TO CUSTOMER
SYSTEM TEST

Components Test

1. Evaluate devices: Review schematics, design rules, process characteristics, vendor test procedures, in process controls, vendor measured characteristics.
2. Characterize devices: Define optimum reliable area of operation (widest operating margins). The process takes 3 to 6 months.
3. Generate test specifications: Specifications written around operating margins as defined by component characterization.
8. 100% temperature screen test: Component is exercised under full voltage margins at 70°C ambient.

System Test

9. Single card test to meet specifications: Use fully loaded card tested in macrodata 100 to verify if board is operational and satisfies margins at room temperature.
10. Multiple card test at maximum specification ambient: Boards are tested for a minimum of 24 hours (must run error tree) at 70°C.
11. Visual inspection and documentation: Visual check of workmanship and check for completness of documentation.

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel. (408) 737-5000
Telex 910-339-9240

National Semiconductor GmbH
Industriestraße 10
8080 Fürstenfeldbruck
West Germany
Tel. 08141/103-1
Telex 05-27649

National Semiconductor (UK) Ltd.
Larkfield Industrial Estate
Greenock, Scotland
Tel. 0475-33251
Telex 778632

EUROPEAN SALES OFFICES

BELGIUM
NATIONAL SEMICONDUCTOR
789 Ave. Houba de Strooper
1020 Bruxelles
Tel. 02-478-3400
Telex 61007 Natsem B

FRANCE
NATIONAL SEMICONDUCTOR SARL
Expansion 10000
28, rue de la Redoute
92-260 Fontenay aux Roses
Tél. 660.81.40
Telex NSF 25956 F +

WEST GERMANY
NATIONAL SEMICONDUCTOR GMBH
Cosimastraße 4/1
8000 München 81
Tel. 089/915027
Telex 05-22772

NATIONAL SEMICONDUCTOR GMBH
Ferdinandsplatz 11
6380 Bad Homburg
Tel. 06172/23011
Telex 415887

BRITAIN
NATIONAL SEMICONDUCTOR (UK) LTD.
19 Goldington Road
Bedford
Tel. 02234-211262
Telex 826209

ITALY
NATIONAL SEMICONDUCTOR SRL
Via Alberto Mario 26
20149 Milano
Tel. (02) 4692864/4692431
Telex 36540

NATIONAL SEMICONDUCTOR GMBH
Hohenheimerstraße 11
7022 Leinfelden-Stuttgart
Tel. 0711/751057
Telex 7255746

DENMARK
NATIONAL SEMICONDUCTOR LTD.
Vodroffsvej 44
1900 Copenhagen V
Tel. 01-356533
Telex 15179 nsc dk

SWEDEN
NATIONAL SEMICONDUCTOR AB
Algrytevagen 23
S-127 32 Skarholmen
Tel. 08-970835
Telex 10731

NATIONAL SEMICONDUCTOR GMBH
Dockenhudener Straße 29
2000 Hamburg 55
Tel. 040/868457
Telex 211039

©1977 NATIONAL SEMICONDUCTOR CORP IM-CP70M17/PRINTED IN W-GERMANY